TIME DOMAIN ANALYSIS OF MICROWAVE NONLINEAR CIRCUITS

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CERTIFICATE

This is to certify that the work presented in this thesis titled, *"Time domain analysis of microwave nonlinear circuits"* has been carried out by G.Bhaskar under my supervision and the same has not been submitted elsewhere for a degree.

Dated : 7th Aug. 1989

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To my mother and father

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My sincere thanks are due to all of my friends who made my stay here a memorable one.

ABSTRACT

Solid state microwave components are all nonlinear to some degree. The circuit analysis of these components requires a nonlinear device model and analytic means to extract the effect of device-circuit interactions. The two main techniques used for the nonlinear circuit analysis are frequency-domain and time-domain techniques. The frequency-domain simulation can be applied to circuits having weak nonlinearity and also these techniques takes excessive amount of time if the circuit has a large number of harmonics.

This thesis work presents a time-domain technique for solving a class of strongly nonlinear microwave circuits or input signals having a large number of harmonics. The entire circuit is discretized in time domain, by Backward-Euler numerical technique. Equivalent circuit models have been used for capacitor and inductor in each time step resulting in a set of nonlinear equations. In the standard methods available for circuit analysis such as SPICE, these equations are solved iteratively. At each time step, these equations are linearized using Newton-Raphson method and solved by matrix inversion. This leads to a large number of matrix inversions and linearizations of the equations, one for each iteration.

In the present analysis, a procedure has been developed which reduces the computational time significantly by solving the nonlinear equations directly, using a new iteration procedure. An assumed set of initial node voltages are iteratively updated according to an error criteria, based on the difference between the assumed and the calculated node voltages.

This procedure involves only one matrix inversion per time step. However, the convergence of the iterartive process requires that the sum of the absolute values of the elements of any row or column vectors of the system Jacobian matrix be less than or equal to one. This condition can be satisfied by choosing a proper time step. In the present study proper time step for convergence has been arrived at

experimentally.

The method has been applied to a harmonic converter circuit. Equivalent circuit model for Schottky diode, step recovery diode and lossy dispersive transmission line also have been discussed in this thesis work.

CONTENTS

1.INTRODUCTION

1.1 *Introduction*

The trend toward monolithic integration of microwave circuits is intensifying interest in computer-aided design. The interest is predominantly in the analysis and design of microwave circuits containing nonlinear devices. The optimum design of microwave circuits containing nonlinear solid state devices requires an accurate technique for predicting their performance. The techniques used for the nonlinear circuit analysis can be classified mainly into two categories, viz., frquency-domain and time-domain techniques.

1.2 *Frequency-domain methods*

In frequency-domain techniques, as the name itself suggests, the solution to the circuit problem is effected in the Fourier transform domain. In the transformed domain the signal is often represented by its Fourier series with finite number of terms. The time-domain differential equations governing the circuit are converted to nonlinear algebraic equations in the transformed domain using Fourier techniques. These equations are solved for different harmonics using iterative procedures.

The frequency-domain techniques are well suited for linear circuits, especially the distributed components. It is usually possible to find closed form expressions for distributed components in frequency-domain, therefore simulating these components is inexpensive. The active devices are generally nonlinear, and modelling of these components in frequency-domain is difficult. Also these techniques are inefficient if the circuit generates a large number of harmonics or the input has a large number of harmonics.

E.M.Bailey [1] has introduced a frequency-domain technique for nonlinear system, popularly known as Harmonic balance method. In this

method, each current or voltage variable is represented by a Fourier series that satisfies the requirement of periodicity. An optimization algorithm is then used to adjust the coefficients of the Fourier series such that the system equations are satisfied with least error. Its main disadvantage is the large number of variables that must be optimized. Nakhla and Vlach [2] have proposed a method which can reduce the number of variables to be optimized, but the method is efficient only for circuits having few harmonics or weak nonlinearity.

Chua and Ushida [3] have developed algorithm for computing almost periodic steady state response of nonlinear systems with multiple frequencies. Hicks and Khan [4] have introduced a general method for the analysis of microwave circuits which contains a sinusoidal source and one or more nonlinear devices. They have achieved good convergence with this method. This technique cannot be applied to circuits having many input harmonics.

Gilmore [5] has modified the harmonic balance technique by analyzing the linear elements in the frequency-domain and the nonlinear elements in the time-domain, the conversion between the frequency-domain solution of the linear network and the time-domain solution of the nonlinearity is usually accomplished using Fast Fourier Transform techniques. This limits this method to systems having only related signal components.

Lamnabhi [6] has applied Volterra series technique to nonlinear systems. The Volterra series relates the output to the input by a series of convolutions in the time-domain. Unfortunately, Volterra series techniques are restricted to weakly nonlinear systems because of the algebraic complexity of determining Volterra nonlinear transfer functions of high order.

Steer and Khan [7] used a generalized power series expansion of the input-output characteristic of a nonlinear system. This method can be used for multifrequency input systems, but requires modelling of devices in the generalized power series expansion and involves the

evaluation of Jacobian matrix for large number of harmonics.

In general, the frequency-domain techniques are inefficient if the nonlinearity of the circuit is high and/ or input has a very large number of harmonics.

1.3 *Time-domain methods*

The time-domain methods find the voltages and currents in discrete time steps. The system differential equations are converted to algebraic nonlinear equations by numerical technique. The general purpose circuit analysis program like SPICE [8] involves these procedures. The characterization of a nonlinear device by a time-domain model is usually appropriate because circuit models typically relate output parameters to input ones through device physics. The distributed elements are difficult to handle in time-domain, since they are described by partial differential equations.

Silverberg and Wing [9] have proposed a time-domain method for analyzing distributed parameter network containing lumped nonlinear elements. In this method, the linear part of the circuit is described in the frequency-domain and then the description is converted into the time-domain by numerical transform techniques. The solution of the whole network is obtained step by step in time at the interface of the two parts by solving simultaneously the convolution equations for the linear part and the differential equations for the nonlinear part. Because of the inverse-transform calculations, the method is limited to small sized circuits.

1.4 *Present work*

The present work on analysis of microwave nonlinear circuits uses time-domain method for solving a class of microwave circuits having a large number of input harmonics (eg. triangular pulse or step). In SPICE, the nonlinear equations are solved iteratively. The nonlinear equations are linearized using Newton-Raphson numerical technique and

then the equations are solved using matrix inversion. This leads to a large number of matrix inversions per time step. In the present method, the system of nonlinear equations are directly solved using an iteration method, thus reduces the computational time involved in matrix inversions significantly. An assumed set of initial node voltages are iteratively updated according to an error criteria based on the assumed and the calculated node voltages. This method requires only one matrix inversion per time step. However, the convergence of the iterative process requires that the sum of the absolute values of the elements of any row or column vectors of the system Jacobian matrix be less than or equal to one.This conditon can be satisfied by choosing a proper time step.

The method is applied to a harmonic converter circuit. This circuit consists of a sampler and a driver circuit. The sampler circuit uses nonlinear GaAs Schottky diodes as sampling switches. The driver circuit uses a step recovery diode for generating a narrow sharp triangular pulse to drive the sampler circuit.

1.4.1 *Time-domain device modelling*

The characterization of a nonlinear device by a time-domain model is appropriate since the output parameters are related to input ones through device physics. Modelling of GaAs Schottky barrier diode and step recovery diode are considered in the present thesis.

The modelling of GaAs Schottky diode has been reported by Thomas. W. Crowe [10]. He used this model to study conversion loss in a mixer diode. Sussmon fort [11] has developed a SPICE model for GaAs Schottky diode. A simple nonlinear model is used in this thesis. This model takes into account the series element and parasitic elements.

The modelling of step recovery diode has been reported by S.Hamilton [12]. He used a simple idealized model in harmonic generation circuits. The improved physical modelling of step recovery diode has been developed by John.L.Moll and Hamilton [13]. The present model for

step recovery diode include the finite recombination effect,the finite transition time and the series resistance.

1.5 *Organization of the Thesis*

The major contribution of this thesis is an improved time-domain analysis method for nonlinear microwave circuit analysis, which is computationally more efficient and is specially designed for analysing circuits with high order nonlinearity. The method is also capable of handling signals with large number of harmonics.

In chapter 2, the methods of analysis available in the open literature for the nonlinear microwave circuits are reviewed. A more detailed description of the proposed time-domain analysis method is also presented along with a discussion on the convergence criteria of the method.

Modelling of nonlinear devices such as step recovery diode, Schottky diode and distributed elements such as lossy dispersive lines is discussed in chapter 3. It may be noted that a microwave circuit may contain nonlinear devices and linear elements interconnected by transmission line sections which may be dispersive. It is important to be able to incorporate all these types of elements in a microwave circuit analysis software.

An application example is presented in chapter 4 which illustrates the use of nonlinear circuit analysis method in analysing a harmonic converter circuit.

The analysis method developed, enables one to evaluate the performance of a given circuit. However, if one wants to design a circuit with optimum performance, it is desirable to couple an optimization procedure with the analysis program, which automatically

adjust the circuit parameters for best performance. Such an attempt is made in chapter 5. Various aspects of this problem are discussed in some detail.

In the concluding chapter, the work reported in this thesis is summarized. Some suggestions are made regarding the possible scope for further work.

2 ANALYSIS OF GENERAL MICROWAVE NONLINEAR CIRCUITS

2.1 *Introduction*

Nonlinear circuit analysis methods can be classified as frequency-domain, time-domain or hybrid (mixed time and frequency-domain) methods depending on how the linear and nonlinear elements are analyzed. The linear elements including distributed components are easier to analyze in frequency-domain method , whereas the nonlinear elements are easier to simulate in time-domain. The hybrid methods have both these features but these methods require calculation of Fast Fourier Transforms and hence, these methods are limited to harmonically related signal components. A brief discussion of all these methods follows.

2.2 *Frequency-domain analysis*

Harmonic balance method : This method [1] is an extension of the phasor analysis from linear to nonlinear differential equations. The solution of the nonlinear differential equations is assumed to be consisting of a linear combination of sinusoids, which are all harmonically related, making the solution periodic. When this assumed solution is substituted into the system equations, the equations can be factored into a sum of purely sinusoidal terms, then superposition (due to the linearity of addition) and the orthogonality of sinusoids at different harmonics can be exploited to break up the resulting algebraic equations into a collection of simpler nonlinear equations, one for each harmonic. These equations are then solved by finding the coefficients of the sinusoids in the assumed solution that result in the balancing of the algebraic equations at each harmonic.

A nonlinear differential equation has the form,

$$f(x,\dot{x},u)=0 \qquad \ldots(2.1)$$

where $u \in p(T_o)$ is the stimulus waveform, x is the unknown waveform to be found and f is continous and real. $p(T_o)$ denotes the set of all periodic funtions of bounded variation with period T_o, ie. $u \in p(T_o)$ implies that the function u satisfies the Dirichlet-Jordan criterion [17]. Assuming that the solution x exists, is real and belongs to $p(T_o)$, then

$$x(t) = \sum_{k=-\infty}^{\infty} x(k)e^{jk\omega_o t} \quad , \qquad \text{....(2.2)}$$

where $\omega_o = 2\pi/T_o$.

Substituting the assumed solution and its derivative into f, we get the resulting equation as Fourier series,

$$f(x(t),\dot{x}(t),u(t)) = \sum_{k=-\infty}^{\infty} F(X,U,k)e^{jk\omega_o t} \qquad \text{....(2.3)}$$

where $X = [\ldots,X(-1),X(0),X(1),\ldots]^T$

$U = [\ldots,U(-1),U(0),U(1),\ldots]^T$

$$U(t) = \sum_{k=-\infty}^{\infty} U(k)e^{jk\omega_o t}.$$

Finally the system of nonlinear equations have to be solved for X.

$$F(X,U,k) = 0 \quad \text{for all } k \qquad \text{....(2.4)}$$

To show how harmonic balance would be applied to circuit analysis, cnsider a circuit consisting of only voltage-controlled nonlinear resistors and capacitors, linear elements (lumped or distributed), and independent current sources. Assuming that the circuit has a periodic steady state solution and if the circuit has N nodes, then it can be described by

$$f(v,t) = i(v(t)) + \frac{d}{dt}q(v(t)) + \int_{-\infty}^{t} y(t-\tau)v(\tau)d\tau + i_s(t) = 0 \quad \text{....(2.5)}$$

where t is the time; v is the vector of node voltage waveforms; i_s is the

vector of source currents; i,q are differential functions representing, respectively, the sum of currents entering the nodes from the nonlinear resistors, and the sum of charges entering the nodes from the nonlinear capacitors; y is the impulse response matrix of the circuit with the nonlinear devices removed; and f is the function that maps the node voltage waveforms into the sum of the currents entering each node.

It is necessary to transform both $f(v)$ and v into the frequency-domain. To make the problem numerically tractable, the number of harmonics considered has to be some finite number.

Since y is linear, the Laplace transform may be used to transform it into the frequency-domain $y \longleftrightarrow Y$. Also, since v is periodic and the circuit is stable

$$\int_{-\infty}^{t} y(t-\tau)v(\tau)d\tau \longleftrightarrow YV$$

where V contains the Fourier Coefficients of the voltage at each node and for each harmonic and Y is a block node admittance matrix for the linear portion of the circuit..

$$Y = [Y_{mn}] \qquad m,n \in \{1,2,\ldots N\}$$
$$Y_{mn} = [Y_{mn}(k,l)] \qquad k,l \in \{0,1,\ldots,H-1\}$$

where m,n are the node indices; k,l are the frequency indices.

$$Y_{mn}(k,l) = \begin{cases} Y_{mn}(jk\omega_0) & \text{if } k = l \\ 0 & \text{if } k \neq l \end{cases}$$

Now, equation (2.5) can be transformed into the frequency-domain,

$$F(V) = I(V) + j\Omega Q(V) + YV + I_S = 0 \qquad \ldots(2.6)$$

where I_S is the Fourier Transform of i_S. Similarly, F(V), I(V), Q(V) are the Fourier Transforms of f(v), i(v), q(v) respectively.

$$\Omega = [\Omega_{mn}], \qquad m,n \in \{1,2,\ldots,N\}$$

$$\Omega_{mn} = \begin{cases} \text{diag}\{0,\omega_0,\ldots,(H-1)\omega_0\}, & m = n \\ 0, & m \neq n. \end{cases}$$

The nonlinear equations (2.6) have to be solved for each harmonic to determine the Fourier coefficients of the voltage at the each node.

2.3 *Hybrid (or mixed frequency and time-domain) method*

This method uses time-domain for nonlinear portion of the circuit and frequency-domain for linear portion of the circuit. A given circuit is partitioned into subcircuits, one subcircuit consisting of linear elements and the other one consisting of nonlinear elements only. The N branches of the linear-nonlinear interface connect the two subcircuits and define corresponding nodes. The current flowing out of the linear circuit must equal flowing into the other. Matching the frequency components in each branch satisfies the continuity equation for current (fig 2.1).

The nonlinear circuit is represented by a set of nonlinear equations,

$$i_J(t) = g(v_1(t),\ldots,v_N(t)) \qquad \ldots(2.7)$$

where g is an arbitrary nonlinear function and i_J and v_J are the Jth branch current and voltage respectively.

The linear circuit is represented by an N by (N+M) matrix, obtained by standard linear circuit analysis. The M additional variables are the additional external nodes at which applied voltages (or currents) are present. The linear circuit matrix is calculated at each

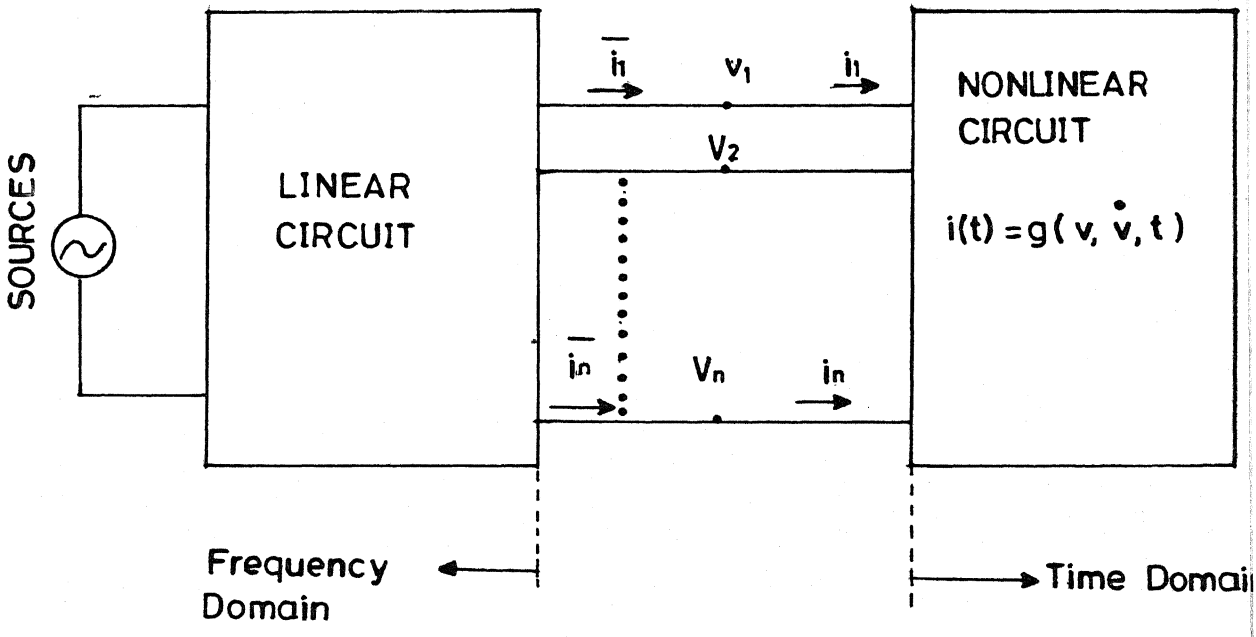


Fig. 2.1 Analysis of Nonlinear Circuit by Hybrid Method.

frequency component in the circuit. This matrix is

$$\begin{bmatrix} V_1(k\omega) \\ \vdots \\ V_N(k\omega) \end{bmatrix} = \begin{bmatrix} H_{11}(k\omega) & H_{12}(k\omega) & \cdots & H_{1(N+M)}(k\omega) \\ & & \vdots & \\ H_{N1}(k\omega) & H_{N2}(k\omega) & \cdots & H_{N(N+M)}(k\omega) \end{bmatrix} \begin{bmatrix} \bar{i}_1(k\omega) \\ \vdots \\ \bar{i}_N(k\omega) \\ V_{N+1}(k\omega) \\ \vdots \\ V_{N+M}(k\omega) \end{bmatrix} \quad \ldots(2.8)$$

where $k = 0,1,2,\ldots,q$ and $H_{ij}(k\omega)$ are the impedance or transfer variables, depending on which of the variables are voltages and which are currents.

The initial guesses are established for the current phasors $\bar{i}_j(k\omega)$ at the interface branches at the dc, fundamental and harmonic frequencies ($k = 0,1,2,\ldots,q$). The hybrid matrix for the linear circuit $H(k\omega)$ is calculated at dc, the driving frequency ω, and each harmonic. This is used with $\bar{i}_j(k\omega)$ and the applied voltages in equation (2.8), to calculate the unknown phasor components of voltages at each of the N branches.

Then using an expression,

$$v_j(t) = \mathrm{Re} \sum_{k=0}^{q} v_j(k\omega)\, e^{jk\omega t} \quad \ldots(2.9)$$

to derive the time values of the branch voltages at times $t = T_S, 2T_S, \ldots$ and a similar expression for derivatives, the time samples of voltage and its derivatives are calculated at each of the N nodes.

The values of $i_j(t)$ in the nonlinear side of the interface branches are obtained at corresponding time instants by substitution of the time samples of the voltage $v_j(t)$ and its derivatives into eqn.(2.7) .

Using the DFT, the harmonic phasor components $i_j(k\omega)$ can be extracted.

An error function is formed to compare the 'nonlinear' current estimates i_j with the 'linear' estimates $\bar{i}_j$,

$$E(i_1,i_2,\ldots i_N,\bar{i}_1,\bar{i}_2,\ldots,\bar{i}_N) = \sum_{k=0}^{Q}\left[|i_1(k\omega) - \bar{i}_1(k\omega)|^2 + \ldots |i_N(k\omega) - \bar{i}_N(k\omega)|^2\right] \qquad \ldots(2.10)$$

The error function is then minimized by forming new guesses for the current phasors $\bar{i}_j(k\omega)$ from the old estimates, and repeating the above procedures until the error function lies below some threshold value (near zero). The fixed point method of Hicks and Khan [4] is used to force the error function to zero, by allowing the phasor currents to more closely approximate their true values on successive iterations. After rth iteration process, the current in the jth branch is

$$i_{jr}(t) = \sum i_{jk}(k\omega)\, e^{jk\omega t}$$
$$\bar{i}_{jr}(t) = \sum \bar{i}_{jk}(k\omega)\, e^{jk\omega t}$$

The next iteration is then carried out with $\bar{i}_{j(r+1)}(k\omega)$ formed by

$$\bar{i}_{j(r+1)}(k\omega) = p\, i_{jr}(k\omega) + (1-p)\,\bar{i}_{jr}(k\omega) \qquad \ldots(2.11)$$

where p is determined by convergence considerations and $0<p\leq 1$.

2.4 Time-domain analysis

The time-domain method analyze the circuits at discrete time steps. The voltages and currents are described by a set of points over

ther period obtained at discrete time instants. The time-domain method involves the following steps.

i) Converting the nonlinear differential equation into nonlinear algebraic equation by numerical integration of time equation.

ii) Formulating the system matrix equations using standard circuit analysis such as nodal analysis, Tableau approach.

iii) Solving the system equations by linearizing them.This nonlinear iteration process is repeated until convergence occurs.

iv) The whole procedure is repeated for all time steps.

Any time domain method uses the following algorithm:

Algorithm: (Time incremental circuit analysis.)

Input: Circuit description, Maxtime

Output: Voltages, currents as functions of time.

Start

Nowtime = 0

Repeat (Time loop)

Repeat (Nonlinear loop)

Stamp circuit elements into matrix 'A' and 'B'

Solve linear system AX = B.

Until Nonlinear loop converged.

Write (Nowtime, X(Nowtime))

Nowtime = Nowtime + Δt

Until Nowtime = Maxtime

End.

The circuit equations can be formulated as a system of differential equations

$$f(x,\dot{x},t) = 0 \qquad \text{...(2.12)}$$

where x is a vector of N circuit variables, and t is the time.

The time-domain approach consists of discretizing the time interval into time points t_k, k = 1,2,..., M and by replacing $\dot{x}$ at each time point by an integration formula. Usually backward differentiation formula is used. This approximate $\dot{x}(t_{k+1})$ as a function of x at the previous time points,

$$\dot{x}_{k+1} = \frac{\sum \alpha_p x_{k+1-p}}{h} \qquad ...(2.13)$$

where x_{k+1} is the computed value of $x(t_{k+1})$, $h = t_{k+1} - t_k$ is the integration step size at time t_k and P is the approximation order of the differentiation formula. The integration coefficient α_p are chosen such that $x_k = x(t_k)$, k= 1,2,...,K, when the solution $x(t_k)$ is a polynomial of degree P. For example, the Backward-Euler formula is obtained by choosing P=1, α_0=1, α_1=1 for fixed time steps. By combining equations (2.12) and (2.13), the circuit equations can be expressed as

$$g(x_{k+1}, t_{k+1}) = 0 \qquad ...(2.14)$$

which is a set of nonlinear algebraic equations. This new set of equations has to be solved at every time step to compute x_{k+1}.

General purpose circuit analyzers like SPICE solve the nonlinear system of equations by the Newton-Raphson algorithm at each time step. This uses linearized equivalent circuit numerical models obtained from Newton-Raphson algorithm for nonlinear elements in each time step. The Newton-Raphson algorithm constructs a sequence of vectors x_{k+1}^{j} which eventually converges to x_{k+1}. The vectors x_{k+1}^{j} are the solutions of the set of linear equations:

$$A_{k+1}^{j} \; X_{k+1}^{j} = B_{k+1}^{j} \qquad ..(2.15)$$

where the coefficient matrix A_{k+1}^{j} and the vector B_{k+1}^{j} are related to the jth Newton-Raphson iteration at the time point t_{k+1}. At the each Newton-Raphson iteration process,the coefficient matrix' A_{k+1}^{j}, changes

and hence the matrix A has to be inverted in each iteration ,to get X_{k+1}^{j}. These several matrix inversion per time step can be avoided if we can solve the system of nonlinear equations directely.The direct nonlinear iteration process used in this thesis is explained in section 2.4.2.

2.4.1 *Formulation of nodal admittance matrix and equivalent current source vector*

The nodal analysis is used to formulate the system matrix from circuit equation as

$$[\,A\,][\,V\,] = [\,B\,] \qquad ..(2.16)$$

where V is a set of node voltages, A is a node admittance matrix and B is a equivalent current source vector.Only linear resistors,linear capacitors,linear inductors,voltage and current sources and two terminal nonlinear elements are considered here.

Linear resistor : If 'i' is the positive node and 'j' is the negative node of a resistor of value R,then

$$\begin{aligned} A(i,i) &= A(i,i) + 1/R \\ A(i,j) &= A(i,j) - 1/R \\ A(j,i) &= A(j,i) - 1/R \\ A(j,j) &= A(j,j) + 1/R \end{aligned} \qquad ..(2.17)$$

If one of the nodes, say 'i' is connected to a voltage source, then

$$\begin{aligned} A(j,j) &= A(j,j) + 1/R \\ B(j) &= B(j) + V_S/R \end{aligned} \qquad ..(2.18)$$

where V_S is the voltage source at the corresponding time instant.

Linear capacitor : The Backward-Euler alforithm for solving the first

order differential equation v' = f(v) with a step size h is given by

$$v_{n+1} = v_n + h\, f(v_{n+1}) = v_n + h\, v'_{n+1} \qquad ..(2.19)$$

where v' denotes differentiation with respect to time. For a linear capacitor,

$$v'(t_{n+1}) = i(t_{n+1})/C$$

If we approximate the exact solutions $v'(t_{n+1})$ and $i(t_{n+1})$ by v'_{n+1} and i_{n+1} respectively, then

$$v'_{n+1} = i_{n+1}/C \qquad ..(2.20)$$

Substituting eqn.(2.20) in (2.19), we have

$$i_{n+1} = Cv_{n+1}/h - Cv_n/h \qquad ..(2.21)$$

This relationship can be represented by the equivalent linear port shown in fig. 2.2.(i) with port current i_{n+1} and port voltage v_{n+1}.The value of R remains fixed (assuming fixed step size), the current source depends on the voltage v_n, which is determined during the preceding time step.

Linear inductor : The Backward-Euler numerical algorithm for solving first order differential equation i'=f(i) with a step size h is given by

$$i_{n+1} = i_n + hf(i_{n+1}) = i_n + hi'_{n+1} \qquad ...(2.22)$$

For a linear inductor , v(t) = L i'(t)
and this can be approximated by

$$i'_{n+1} = v_{n+1}/L \qquad ...(2.23)$$

Substituting Eqn(2.23) in (2.22), we have,

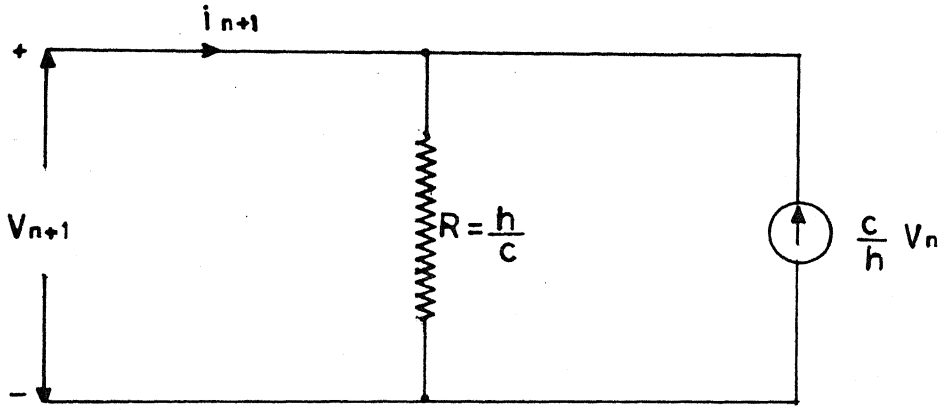


Fig. 2.2(i) Discrete Circuit Model Associated with B-E Algorithm for a Linear Capacitor.

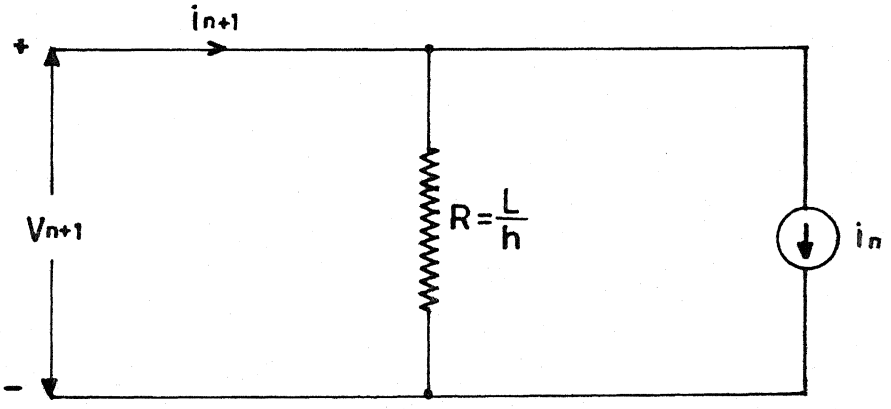


Fig. 2.2(ii) Discrete Circuit Model Associated with B-E Algorithm for a Linear Inductor.

$$i_{n+1} = hv_{n+1}/L + i_n \qquad \text{...(2.24)}$$

This eqn. can be represented by a linear equivalent one port shown in Fig. 2.2(ii). This circuit is the discrete circuit model associated with the B-E algorithm for a linear inductor.

Current Sources : If the current is directed from node, i to j, then,

$$B(i) = B(i) - I_S$$
$$B(j) = B(j) + I_S \qquad \text{...(2.25)}$$

where I_S is the value of the current source.

Nonlinear two terminal elements : The nonlinear elements are characterized by

$$i = f(v,\dot{v},t) \qquad \text{...(2.26)}$$

where v is the voltage across the device and the dot denotes differentiation with respect to time. This can be considered as a current source if the value of the voltage across the device is assumed in each iteration process.

The formulated system of equations has the form

$$[\,A\,][\,V\,] = [\,B\,]$$

if a fixed time step is chosen, then, V can be written as

$$[\,V\,] = [\,A\,]^{-1}\,[\,B\,] \qquad \text{...(2.27)}$$

where A^{-1} is the constant matrix for a fixed time step and B a vector matrix function of nonlinear node voltages. This equation is then solved using direct iteration process, discussed in the following section.

2.4.2 Iteration method

The set of nonlinear equations obtained from numerical integrations can be written as

$$V_1 = \phi_1(V_1, V_2, \ldots V_n)$$
$$V_2 = \phi_2(V_1, V_2, \ldots V_n)$$
$$\vdots \qquad\qquad \vdots$$
$$V_n = \phi_n(V_1, V_2, \ldots V_n)$$

or can be written as

$$[\, V \,] = [\, \phi(V) \,] \qquad \ldots(2.28)$$

where V is the node voltage vector and ϕ is the nonlinear function of node voltages.

A direct iteration method is used to find the actual root of the equations(2.28).The iteration process is

$$x^{(n+1)} = \phi(\, x^{(n)}) \quad , \quad (n=0,1,2,\ldots) \qquad \ldots(2.29)$$

If this process of iteration converges ,then the limiting value is defininitely a root of the equation.(2.29).Let x=X be the solution of the equation and let $x_n = X + \xi_n$, where ξ_n is the error in x_n.By expanding the right hand side of eqn.(2.29) in a Taylor's series,we have,

$$\xi_{n+1} = a_1\xi_n + a_2\xi_n^2 + \ldots\ldots\ldots\ldots ,$$

where $$a_k = \frac{\phi^{(k)}(x)}{k!} \qquad \ldots(2.30)$$

If $a_1 \neq 0$, then the errors ξ_n, resulting from the successive repetitions of the iteration process are re lated by

$$\xi_{n+1} = a_1\xi_n \; ; \quad \xi_{n+m} = a_1^m\xi_n$$

The criteria for the convergence of the process is that $|a_1| = |\phi'(x)|$ must be less than one,and the magnitude of the error decreases exponentially with' n' increasing.

We can make a better approximation to the initial guess in the process of iteration by 'exponential extrapolation'.If we consider only the first term in the Taylor's series expression(2.30),then

$$\varepsilon_2/\varepsilon_1 = \varepsilon_1/\varepsilon_0 = a_1,$$

or $\varepsilon_0\varepsilon_2 = \varepsilon_1^2$

If x_0 is the initial guess and x_1 and x_2 are the successive solutions,then

$$(x_2 - X)(x_0 - X) = (x_1 - X)^2$$

therefore,an approximate root X^* is given by

$$X^* = x_2 - \frac{(x_2 - x_1)^2}{(x_2 - 2x_1 + x_0)} \qquad ...(2.31)$$

This process is repeated with starting $x_0 = X^*$ till convergence is reached.An error function is formed to check for convergence.If x_0 is the initial guess and x_1 is the next iteration solution ,then error function is given by

$$E = \frac{\sum (x_1^{(i)} - x_0^{(i)})^2}{\sum_{i=1}^{N} x_0^{(i)2}} \qquad ...(2.32)$$

where N is the number of nodes.The iteration process is continued till E lies below some threshold value.This limiting value for the iteration process is taken as 0.1% of the x value.

2.4.3 Convergence of the iteration process

The iteration process(2.29) converges if

$$\sum_{j=1}^{n} \left| \frac{d\phi_i(v)}{dv_j} \right| \leq q_i < 1 , \qquad (i = 1,2,....,n)$$

or

$$\sum_{j=1}^{n} \left| \frac{d\phi_j(v)}{dv_i} \right| \leq q_i < 1 , \qquad (i = 1,2,....,n) \qquad ...(2.33)$$

Consider the system of nonlinear equations

$$A(h)\ v = B(v,h)$$

where A is a matrix,function of time step'h',and B is a vector ,function of node voltages and time step.Therefore 'v' can be determined from the above equation as

$$[\ V\ ] = [\ A\ ]^{-1}\ [\ B\ ] = [\ C\ ]\ [\ B\ ] \qquad ...(2.34)$$

where C is the inverse of A.Now, v can be written in expanded form as,

$$[\ V\ ] = \begin{bmatrix} C_{11}b_1 + \ldots\ldots\ldots + C_{1n}b_n \\ \vdots \\ C_{n1}b_1 + \ldots\ldots\ldots + C_{nn}b_n \end{bmatrix} = \begin{bmatrix} \phi_1(v,h) \\ \vdots \\ \phi_n(v,h) \end{bmatrix} \qquad ...(2.35)$$

Consider a special case where,only V_1 and V_2 are the node voltages.For this,only b_1 and b_2 are functions of V_1 and V_2 respectively,which are represented as

$$b_1 = f_1(V_1,V_2)$$
$$b_2 = f_2(V_1,V_2)$$

For a diode nonlinear device,

$$b_1 = I_S(\exp\alpha V - 1) + \frac{C_{jo}}{(1-V/\phi)^m} \frac{dV}{dt} \qquad ...(2.36)$$

$$b_2 = -b_1$$

where $V = V_1 - V_2$.

Applying the convergence criteria (2.33),

$$\left|\frac{\partial \phi_1}{\partial V_1}\right| + \left|\frac{\partial \phi_1}{\partial V_2}\right| = \left|C_{11}\frac{\partial b_1}{\partial V_1}\right| + \left|C_{11}\frac{\partial b_1}{\partial V_2}\right| < 1 \qquad \text{...(2.37)}$$

if C_{12} is small.

where

$$\frac{\partial b_1}{\partial V_1} = \alpha I_S \exp(\alpha V) + \frac{C_{jo}}{\Delta t}\frac{1}{(1-V/\phi)^m} + \frac{m(V_n - V_{n-1})C_{jo}}{\phi\,\Delta t\,(1-V/\phi)^{m+1}}$$

$$\frac{\partial b_1}{\partial V_2} = \alpha I_S \exp(\alpha V) - \frac{C_{jo}}{\Delta t}\frac{1}{(1-V/\phi)^m} + \frac{m(V_n - V_{n-1})C_{jo}}{\phi\,\Delta t\,(1-V/\phi)^{m+1}}$$

The following approximations can be made to satisfy Eqn.(2.37) :

(i) Because of the exponential dc characteristic of the diode, the condition (2.37) is sometimes difficult to satisfy. To avoid this, a linear approximation to dc characteristic can be included at some voltage points and/or a piecewise linear model can be included.

(ii) The junction capacitance can be taken as a fixed one, in which case, the capacitive element value goes to the A matrix.

Finally, a proper time step is chosen experimentally to satisfy Eqn.(2.37).

3. MODELLING OF MICROWAVE DIODES AND TRANSMISSION LINES

3.1 *Introduction*

The behaviour of a semiconductor device for a given geometry and doping profile is governed by the device physics, and can be represented by a set of equations. The solution of these equations yields the device characteristic. The terminal characteristic of a device can be modelled by an equivalent circuit consisting of lumped components. The transmission lines have distributed characteristics. Modelling of transmission lines, only by lumped elements is not possible. But distributed components can be modelled in time-domain by many sections of delay elements and lumped elements.

3.2 *Piecewise-Linear modelling*

Most electronic nonlinear device can be realistically modelled by a piecewise-linear characteristic.

A nonlinear voltage controlled two terminal resistor is described by a canonical piecewise-linear represntation [19]. Consider an arbitrary continuous piecewise-linear function 'f' with 'p' distinct break points (fig 3.1). Let m_i,(i = 0,1,...,p) denote the slope of each segment. v_1(v$_2$(...(v$_p$. Then' f' can be described by a canonical form given by

$$i = f(v) = a + bv + \sum_{i=1}^{p} c_i|v-v_i| \qquad ...(3.1)$$

where the coefficients can be calculated explicitly from,

$$b = (m_0 + m_p) / 2$$

$$c_i = (m_i - m_{i-1}), \qquad i = 1, 2,...,p$$

$$a = f(0) - \sum_{i=1}^{p} c_i |v_i|.$$

3.3 *Modelling of GaAs Schottky diode*

The nonlinear nature of a diode can be described by

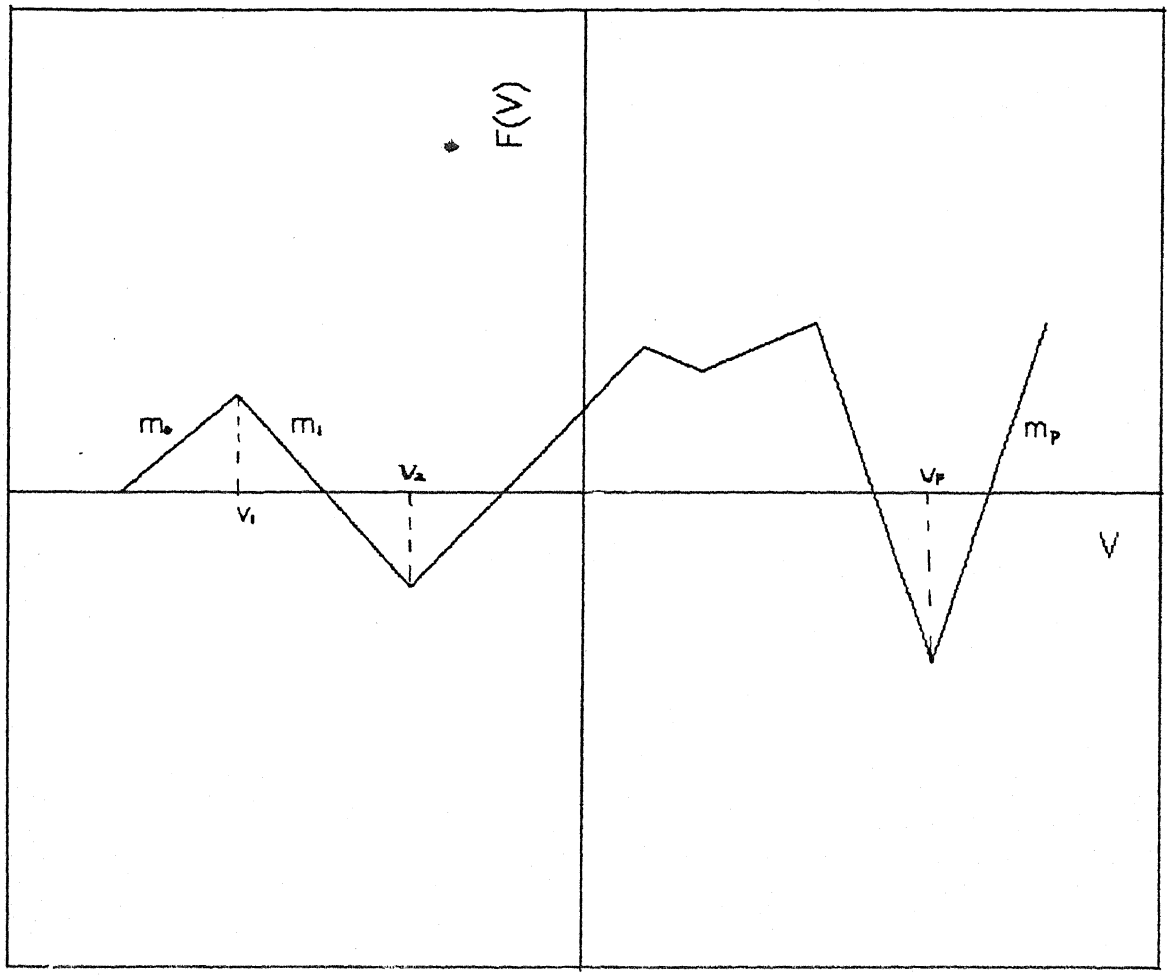


Fig.3.1 Piecewise-linear representation of a nonlinear function

$$i = f(v,\dot{v}) \qquad \ldots(3.2)$$

where v is the voltage across the diode and i is the current through the device and f is a nonlinear function describing the v-i characteristic.

The dc current-voltage characteristic of a GaAs Schottky barrier diode is described by

$$i = I_S [\, e^{v/nv_T} - 1] \qquad \ldots(3.3)$$

where I_S is saturation current, $v_T = KT/q$ and n is the ideality factor. q- electronic charge, K - Boltzmann's constant and T - temperature.

The saturation current is given by Richardson-Dushman equation [24] for the thermionic current,

$$I_S = AA^{*}T^2 \exp(-\phi_b/v_T) \qquad \ldots(3.4)$$

where A - Junction area, A^{*} - Effective Richardson constant, T - temperature, °K, ϕ_b - barrier height in volts.

$$A^{*} = (4\pi m^{*} K^2)/h^3$$

where m^{*} = Effective electron mass, h - Planck's constant.

The depletion or the junction capacitance of a Schottky barrier diode is given by

$$C_j = \frac{C_{jo}}{(1-v/\phi)^m} \qquad \ldots(3.5)$$

where C_{jo} is the zero bias depletion capacitance, v is the applied reverse bias, ϕ is the junction potential and m is the grading

coefficient. m = 1/2 for a step junction.

3.3.1 *Equivalent circuit of Schottky barrier diode*

The equivalent circuit for the GaAs Schottky barrier diode is shown in fig. 3.2(i). R_s is the series resistance, C_p and L_s are the package reactances. The series resistance is a complex function of voltage and frequency and is determined usually by experiments.

To avoid the occurence of overflow because of the exponential characteristic of the device, a linear characteristic tangent to the diode characteristic at some voltage point is included in the model. Similarly a linear characteristic is drawn at some point on the diode reverse bias characteristc to avoid underflow (fig 3.3).

The dc current-voltage charcteristic of a typical GaAs Schottky barrier diode is shown in fig 3.4. The parameters for this diode are I_s=0.75 nA, n = 1.0, v_T = 26.3 mV, vJ = 0.2 V, C_{jo}= 1 pf and R_s = 12 Ω. The c-v characteristic for this diode is shown in fig.3.5.

3.4 *Modelling of step recovery diode*

The idealized equivalent circuit of the step recovery diode shows that the diode behaves as a two state capacitor of large capacitance under forward charge storage and small capacitance under reverse storage, with zero switching time between two states. The forward storage capacitance is the diffusion capacitance of the i layer and reverse capacitance is the depeltion capacitance of the space charge layer.

A first order improvement in the diode idealized model is obtained by accounting for the recombination of the forward stored charge as expressed by the continuity equation. The recombination is a function of the effective minority carrier life-time τ_R. Since forward

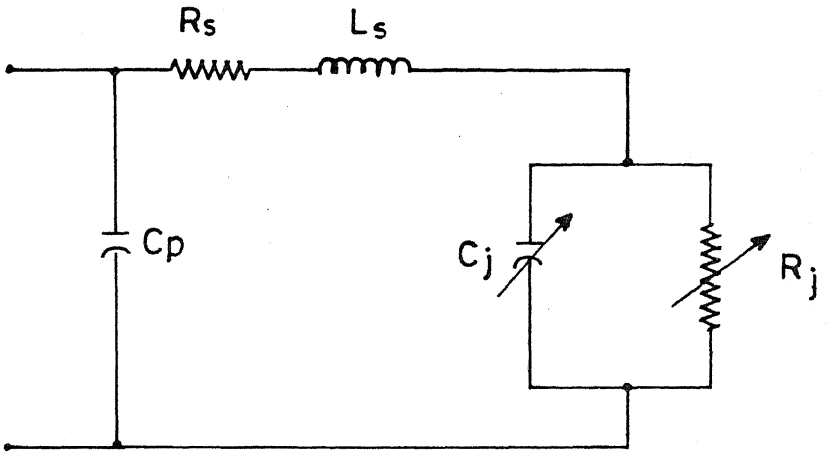


Fig. 3.2 (i) Equivalent Circuit Model of a GaAs Schottky Diode.

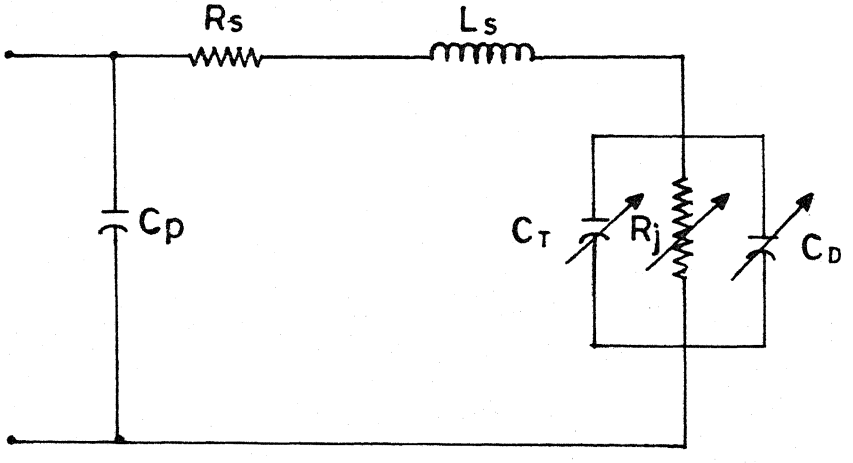


Fig. 3.2(ii) Equivalent Circuit Model of a Step Recovery Diode.

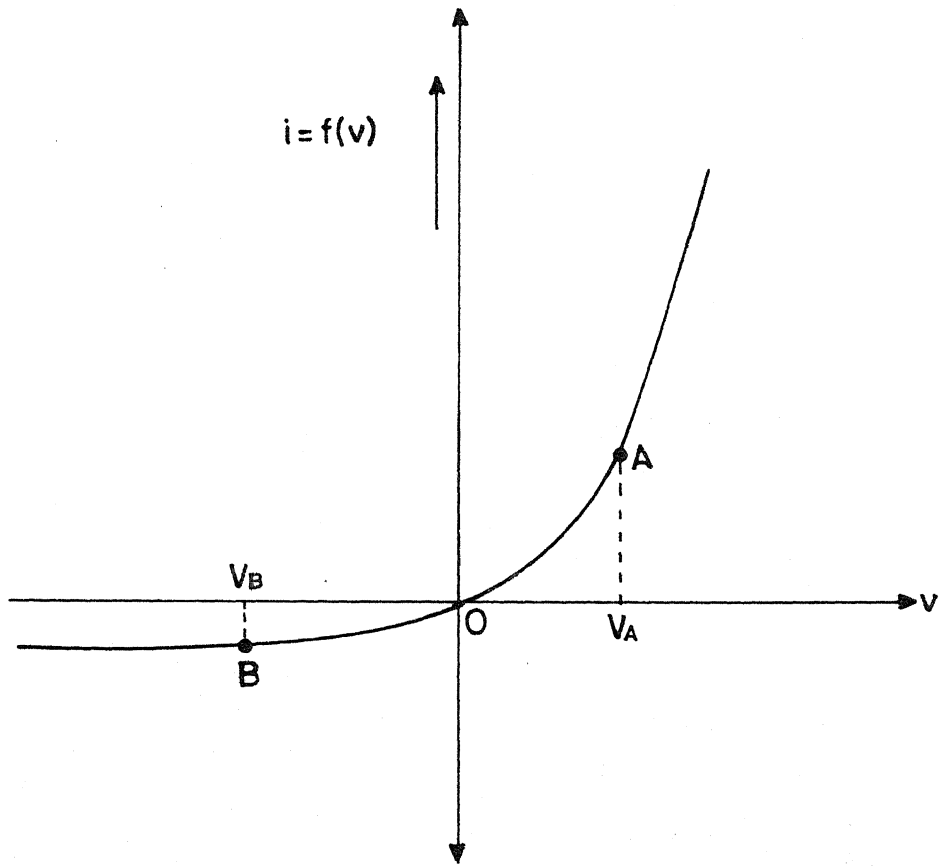


Fig. 3.3 Diode D C Characteristic is Linearized At Points A and B .

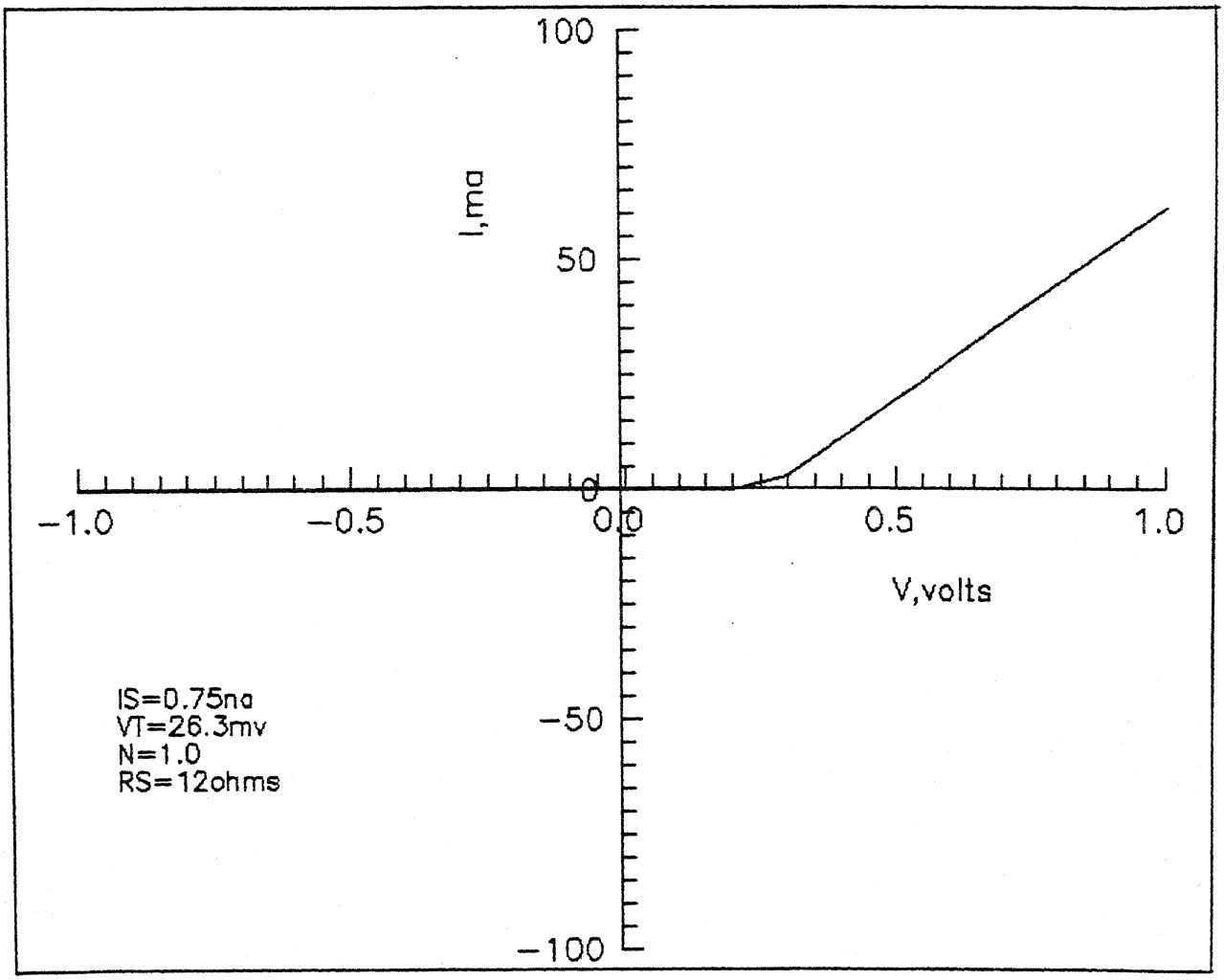


Fig.3.4 i-v characteristic of a GaAs Schottky barrier diode

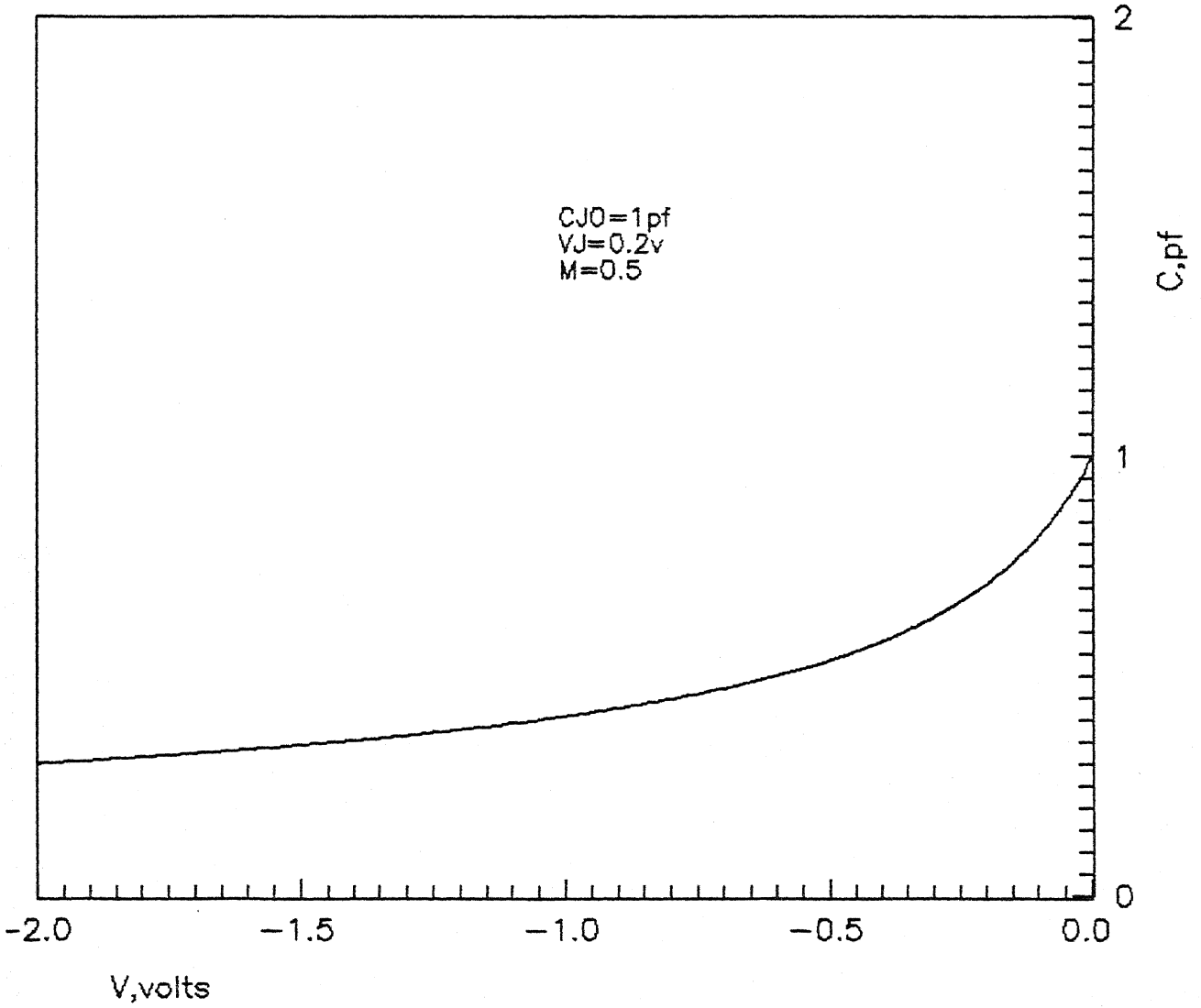


Fig.3.5 c-v characteristic of a GaAs schottky barrier diode

capacitance is determined by having a large number of free carriers there is a finite time constant t_t for switching from forward to reverse capacitance.

In the frequency range $(1/\tau_R) < f < (1/t_t)$, the idealized model is valid. At frequencies lower than $1/\tau_R$, the finite recombination effects must be taken into account and at frequencies higher than $1/t_t$, the effects of finite switching time should be taken into account.

The dc characteristic of a SRD is described by the relation shown in the eqn. (3.3). The saturation current is described by the relationship shown in eqn. (3.4).

The forward diffusion capacitance is modelled as(Appendix-A)

$$C_D = \frac{I_S \tau_R \, e^{v/nv_T}}{nv_T} \qquad \ldots(3.6)$$

and the reverse depletion capacitance is described by

$$C_T = \frac{C_{jo}}{(1-v/\phi)^m} \qquad \ldots(3.7)$$

3.4.1 *Equivalent circuit of SRD*

The equivalent circuit for SRD is shown in fig.3.2 (ii). R_S is the series resistance, L_S and C_p are the package elements. The overflow and the underflow problems are avoided by limiting the exponential characteristic at some point on the diode dc characteristic.

The dc characteristic of a SRD is shown in fig.3.6 and the c-v characteristic is shown in fig.3.7. The parameters for this SRD are I_S = 0.1 * 10^{-15} A, v_T = 26.3 mV, n = 1, m = 0.5, vj = 0.6, C_{jo} = 0.5 pf, τ_R = 10 nS and R_S = 0.8 Ω.

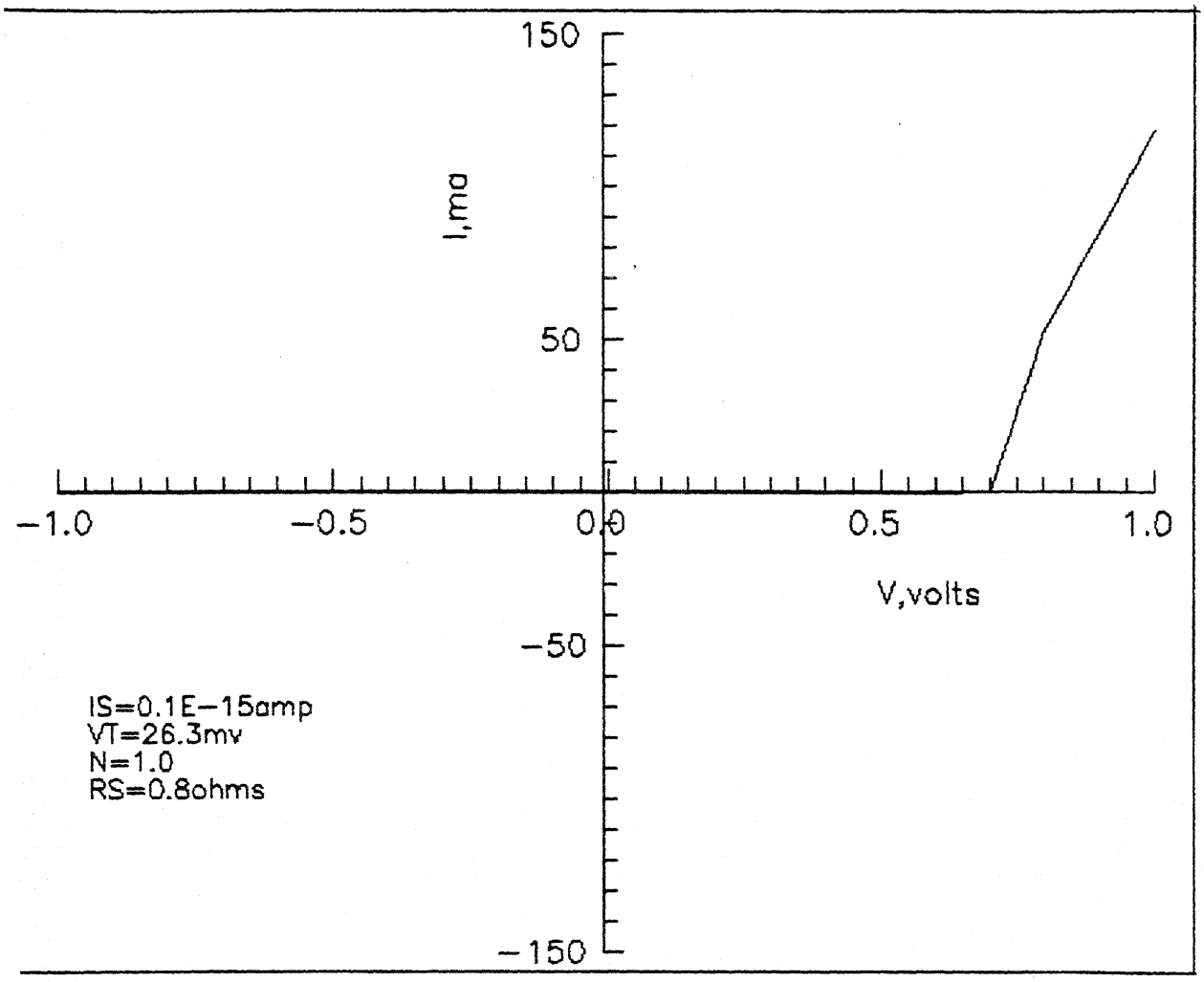


Fig.3.6 i-v characteristic of a step recovery diode

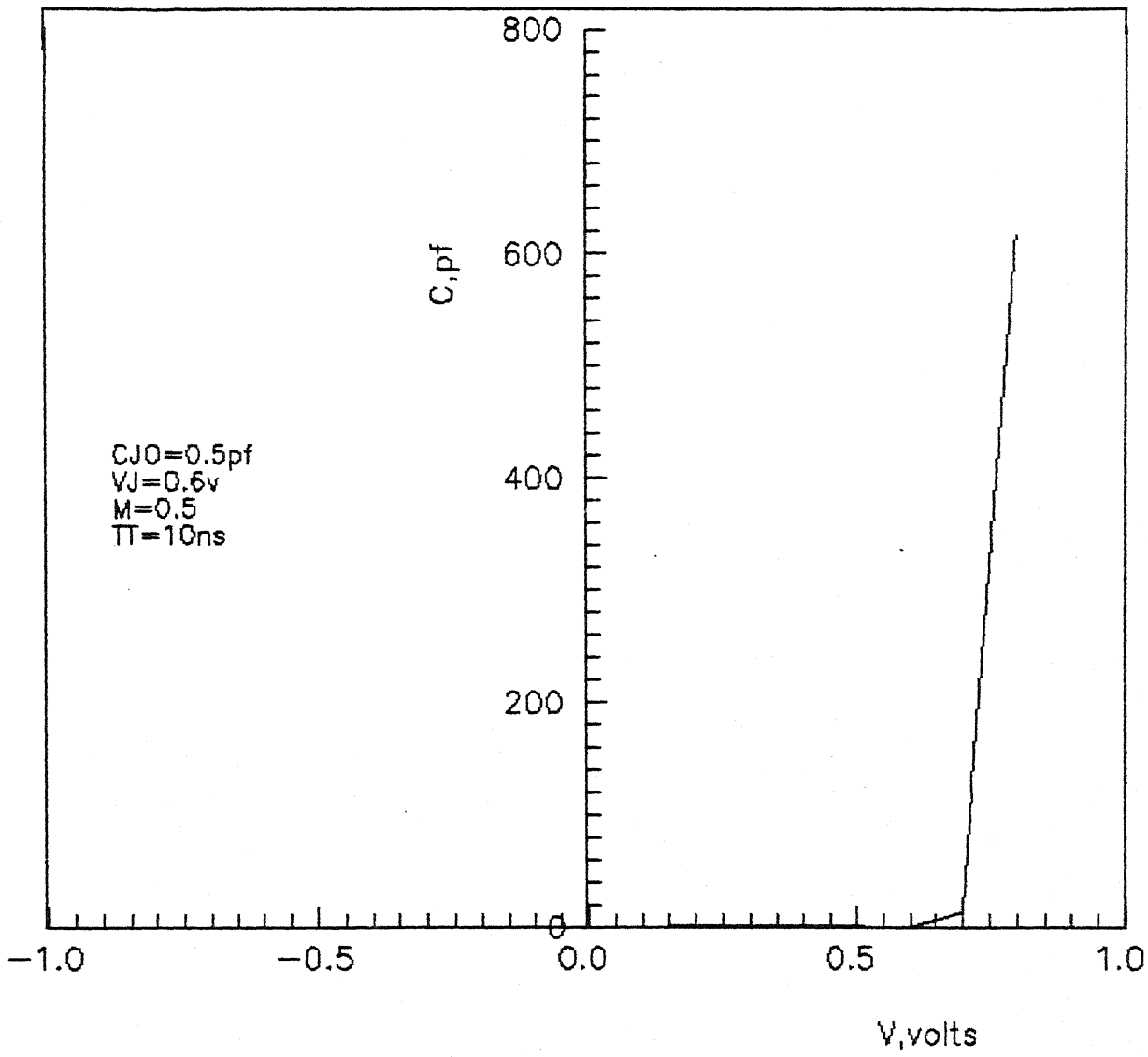


Fig.3.7 c-v characteristic of a step recoverey diode

3.4.2 *Charge storage and reverse transient in SRD*

The large forward capacitance is due to the storage of electrons and holes in the central region of the diode. Not all of the injected charge can be removed because there is carrier recombination in the central layer during the storage period. Fig.3.8 shows the 'step recovery action' when the voltage is abruptly switched from forward to reverse bias.

The total stored charge in the n-side of the diode is

$$Q_S = qA \int_0^{W_n} \Delta p_n dx \qquad \ldots(3.8)$$

where W_n is the n-layer thickness, A is the cross-section of the diode and p_n is the concentration distribution in the n-layer.

The continuity equation for the hole current is

$$\frac{1}{q} \frac{\partial J_p}{\partial x} + \frac{p - p_o}{\tau_p} = - \frac{\partial p}{\partial t} \qquad \ldots(3.9)$$

Multiplying the above equation by qA, we have

$$A \frac{\partial J_p}{\partial x} + qA \frac{\Delta p}{\tau_p} = - qA \frac{\partial p}{\partial t}$$

where J_p is the current density for holes, τ_p is the life time for holes, p_o is the concentration of holes at x=0 and p is the concentration at x.

Integrating eqn.(3.9) from 0 to W_n and using eqn.(3.8) we have

$$I_p(0) - I_p(W_n) = \frac{\partial Q_S}{\partial t} + \frac{Q_S}{\tau_p} \qquad \ldots(3.10)$$

where I_p is the diffusion current for holes and Q_S is the stored charge. Eqn.(3.10) is called the charge control equation. $I_p(W_n)$ is a

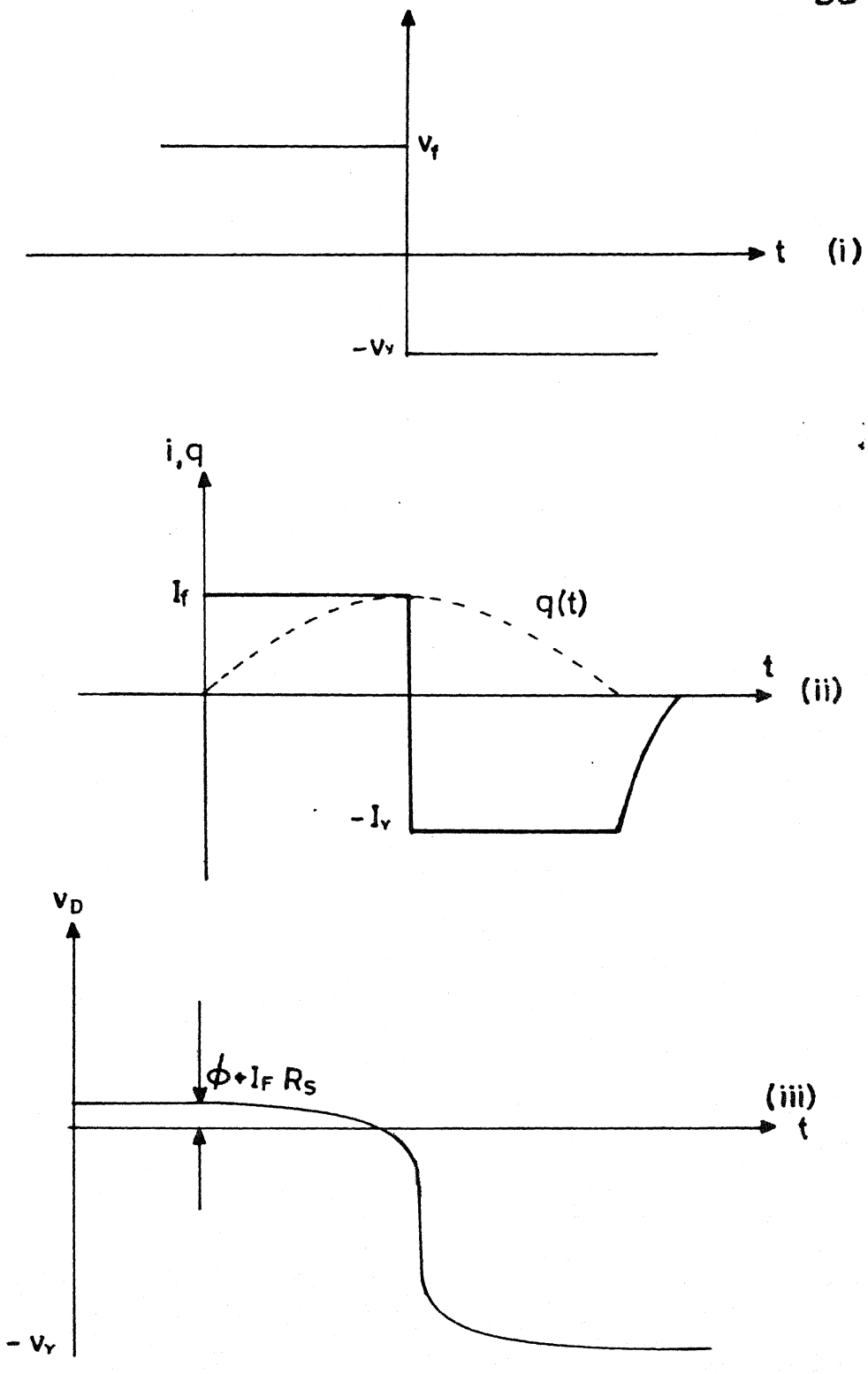


Fig. 3.8 Charge Storage and Reverse Transient in SRD

(i) The Driving Voltage Waveform.
(ii) The Current and Charge Waveform.
(iii) The Diode Voltage Waveform.

small current and can be neglected.

The steady state forward current of the diode is obtained by setting $\frac{\partial Q_s}{\partial t} = 0$,

$$I_f = I_p(0) = \frac{Q_{sf}}{\tau_p}$$

where Q_{sf} is the stored charge under steady state forward bias condition. Thus

$$Q_{sf} = I_f \tau_p \qquad ...(3.11)$$

Now, when a reverse current is applied at t = 0 by reversing the bias voltage as shown in fig.(3.8), the stored charge decays toward zero due to recombination and extraction. The charge control equation then becomes

$$-I_r = \frac{\partial Q_s}{\partial t} + \frac{Q_s}{\tau_p} \qquad ...(3.12)$$

where I_r is the reverse current. Solving this equation with eqn.(3.11) as the initial condition, we get

$$Q_s(t) = \tau_p[- I_r + (I_f + I_r) \exp(-t / \tau_p)] \qquad ...(3.13)$$

The stored charge reaches zero at time t_s(storage time). Therefore using eqn.(3.13) we get t_s as

$$t_s = \tau_p \ln (1+I_f/I_r) \qquad ...(3.14)$$

The recovered charge is given by

$$Q_r = I_r t_s \qquad ..(3.15)$$

and the fraction of the total stored charge that is recovered is then,

$$\frac{Q_r}{I_f \tau_p} = \frac{I_r}{I_f} \ln(1+I_f/I_r) \qquad ..(3.16)$$

If the reverse current is much larger than the forward current, almost all of the stored charge is recovered.

The injected charge to SRD is not completely uniform across the plane of the diode, so the 'fast transition' does not occur across the entire diode simultaneously. An empirical formula [13] for this transition time is given by

$$t_t = [\ 1 - (79.5/V_{BR}f_O)\ ]^2\ t_S + V_{BR} \cdot 10^{-12}/2.5 \qquad ...(3.17)$$

where V_{BR} is the breakdown voltage in volts, t_S is the delay time in sec and f_O is the output frequency in GHz. This turn-on time is much faster than turn-off, so it has been neglected in the model.

3.5 *Modelling of lossy dispersive transmission lines*

The analysis and design of microwave circuits consisting of transmission lines can be facilitated by the use of equivalent circuits. The propagation characteristic, that is, the propagation constant and the impedence of ideal closed waveguides can be modelled in terms of a transmission line or a distributed parameter circuit consisting of LC elements. For ideal structures the series impedence and shunt admittance per unit length of the equivalent distributed parameter structures are rational functions and hence are easily realized in terms of LC elements. This, however, is not the case for open structures such as microstrips. Accurate evaluation of the propagation characteristic of these structures including dispersion, losses and impedance requires numerical techniques. The modelling of lossy dispersive transmission line is reported by V.K.Tripathi [20]. He has developed equivalent circuits for lossy dispersive lines, which consist of ideal lumped linear elements and lossless TEM transmission lines.

The equation describing non TEM lines are

$$-\frac{\partial v}{\partial z} = L(f)\frac{\partial i}{\partial t} + R\,i$$

$$-\frac{\partial i}{\partial z} = C(f)\frac{\partial v}{\partial t} + G\,v \qquad \text{...(3.18)}$$

where L,C,R and G are elements per unit length of the line.

The lossy dispersive transmission line and its equivalent circuit are shown in fig.3.9 (a) and (b). In order to derive the expression for the series impedence, shunt admittance and the parameters of the ideal line, we can make use of ABCD parameters.

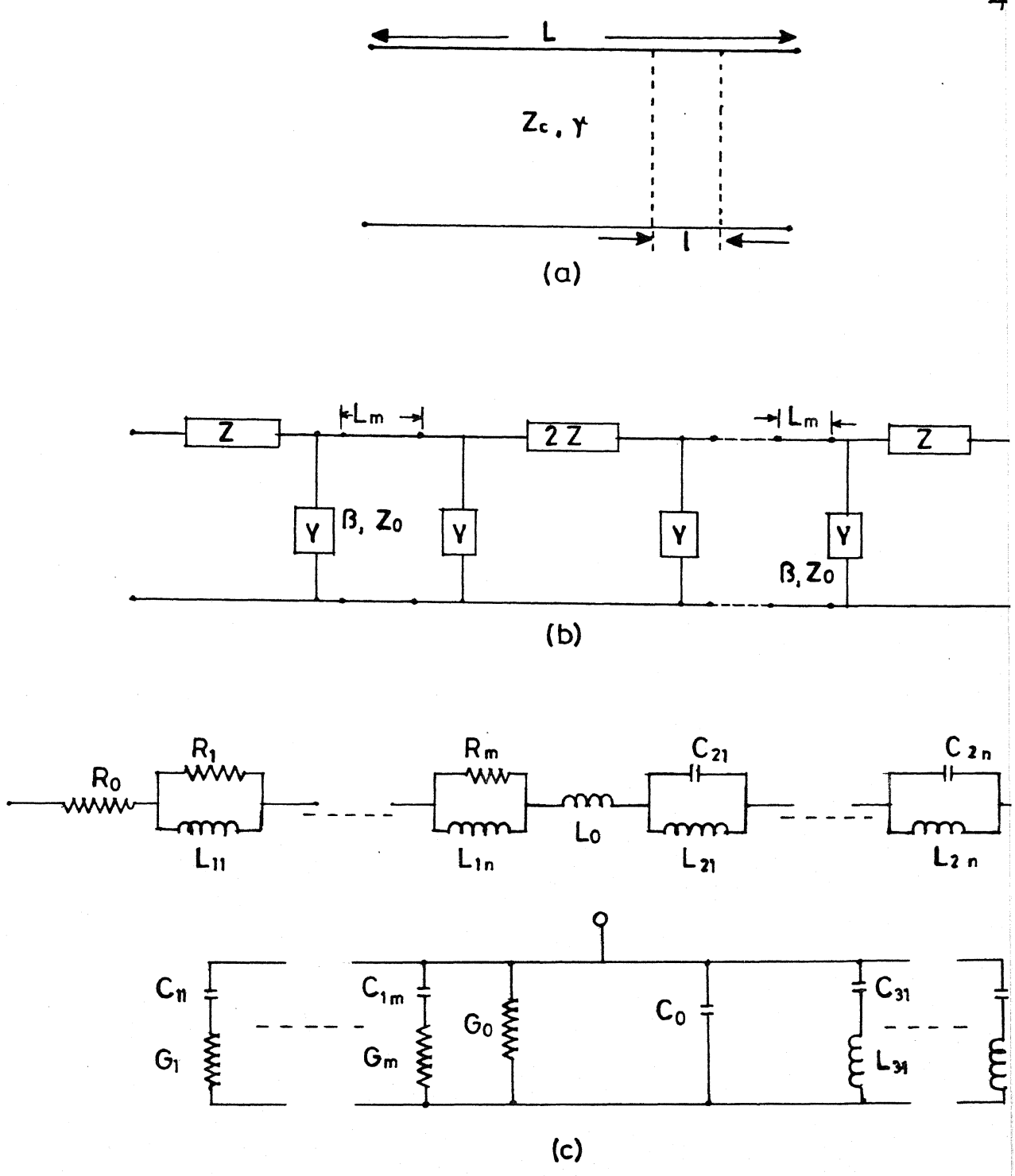
$$(ABCD)_{\text{for the lossy dispersive line}} = \begin{bmatrix} \cosh \gamma l & Z_c \sinh \gamma l \\ \frac{\sinh \gamma l}{Z_c} & \text{Cosh } \gamma l \end{bmatrix} \qquad \text{...(3.19)}$$

where Z_c is the characteristic impedence, γ is the complex propagation constant and l is the length of the line to be modelled. Z_c and γ are functions of frequency.

$$(ABCD)_{\text{for the eq. model}} = \begin{bmatrix} 1+ZY & Z \\ Y & 1 \end{bmatrix} \begin{bmatrix} \text{Cos}\beta_o L_m & jZ_o \sin\beta_o L_m \\ \frac{j\sin\beta_o L_m}{Z_o} & \text{Cos}\beta_o L_m \end{bmatrix} \begin{bmatrix} 1 & Z \\ Y & 1+ZY \end{bmatrix} \qquad \text{...(3.20)}$$

where Z_o, β_o and L_m are the impedance, phase constant and length of the ideal model line, and Z and Y are the series impedance and shunt admittances respectively, of the two terminal lumped networks.

The dispersive line is divided into a number of sections with length l whose maximum value depends on the frequency range of validity of the model and is chosen so that Z and Y are realizable in a desired form. Equating (3.19) and (3.20), [since matrix elements A=D and AD-BC =1], we have



ig. 3.9 (a) Schematic of General Lossy Dispersive Line.
(b) The Equivalent Circuit Model.
(c) General Form of Lumped Circuits for the Series and Shunt Branches in (b).

$$\cosh \gamma l = (1+2ZY)\cos\beta_o L_m + j\,[Z_o Y(1+ZY) + Z/Z_o]\sin\beta_o L_m$$

$$\frac{\sinh\gamma l}{Z_c} = 2Y\cos\beta_o L_m + j\,[1/Z_o + Z_o Y^2]\sin\beta_o L_m \qquad \ldots(3.21)$$

The expressions for the frequency-dependent complex series impedance and shunt admittance branch are derived from the above equations and are given by

$$Z = Z_c \frac{\cosh \gamma l - \sqrt{1+j\sin(\beta_o L_m)\, Z_o \frac{\sinh\gamma l}{Z_c}}}{\sinh\gamma l}$$

$$Y = \frac{j\cos(\beta_o L_m) - j\sqrt{1+j\sin(\beta_o L_m)\, Z_o \frac{\sinh\gamma l}{Z_c}}}{Z_o \sin(\beta_o L_m)} \qquad \ldots(3.22)$$

The model parameters to be determined include the length, the phase constant, and the impedence of the ideal TEM line in addition to the lumped circuits whose driving point impedance and admittance are given by eqns.(3.22).

The lengths of the line to be modelled, l, and the model lossless TEM line, L_m, are chosen such that Z and Y, are realizable in a desired form with ideal RLC elements. The maximum value of the line length to be modelled, depends on the highest frequency at which the structure is to be modelled.

If we choose to realize Z and Y in the general modified Foster form shown in fig.3.9(c), then both functions must be positive real [21] over the desired frequency band for which the model is to be valid. The general form of impedance or admittance to be synthesized in the modified Foster form is given by

$$Z \text{ or } Y = \sum_{i=0}^{N} \left[\frac{jA_i\omega}{(B_i^2 - \omega^2)} + \frac{j\omega D_i}{(C_i + j\omega)} \right] \qquad \ldots(3.23)$$

where the constants A_i, C_i, B_i, D_i in the above equation determine the element values in the model.

4. APPLICATION OF THE TIME DOMAIN METHOD TO THE ANALYSIS OF HARMONIC CONVERTER CIRCUIT

Harmonic converters are used in several microwave measurement systems such as network analysers, frequency counters, sampling oscilloscopes etc, because of their extremely broad band performance. The harmonic converter essentially consists of a sampling gate and a hold circuit, driven by a narrow sampling pulse. Obviously, in order to sample a microwave signal in the GHz frequency range, the drive pulse has to be necessarily much narrower than the period of the microwave signal. For the circuit to work as a down converter one has to choose the drive pulse repetition frequency such that 'n' times the frequency is equal to the signal frequency +IF or -IF frequency. By changing the harmonic number 'n', one can down convert any frequency in a multi octave microwave band with a small variation in the drive frequency. One major difference between the sample and hold circuit used in digitizing a signal at low frequencies and the harmonic converter is that the sampling rate is very much lower than that specified by Shannon's sampling theorem, but satisfies this criteria as far as the base band signal is concerned.

4.1 *Sampling Technique*

Sampling of a signal can be looked at as a multiplication process between the signal and the sampling pulses or the gate conductance function.

$$y(t) = g(t) \cdot x(t) \qquad \ldots(4.1)$$

where $x(t)$ is the microwave signal, $g(t)$ is the conductance of the sampler gate and $y(t)$ is the output of the sampling circuit. Fig. 4.1 (a) and (b) shows the sampling action. The gating signal has a wide frequency spectrum and hence, the sampling circuit has a wide frequency of operation. The sampling action in frequency domain can be modelled as a convolution,

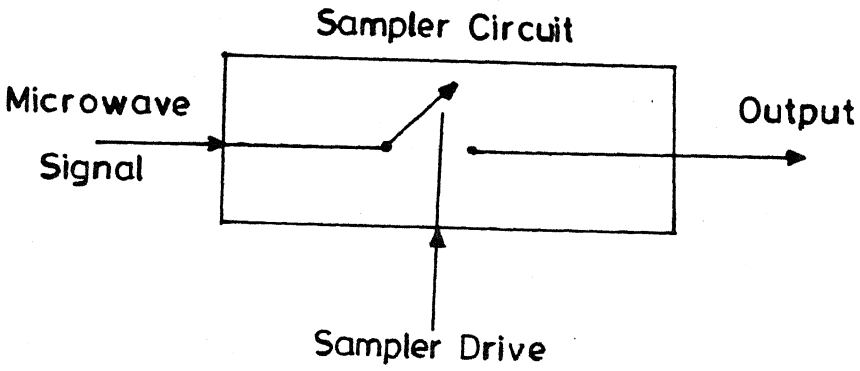


Fig.4.1(a) Sampling by Gating .

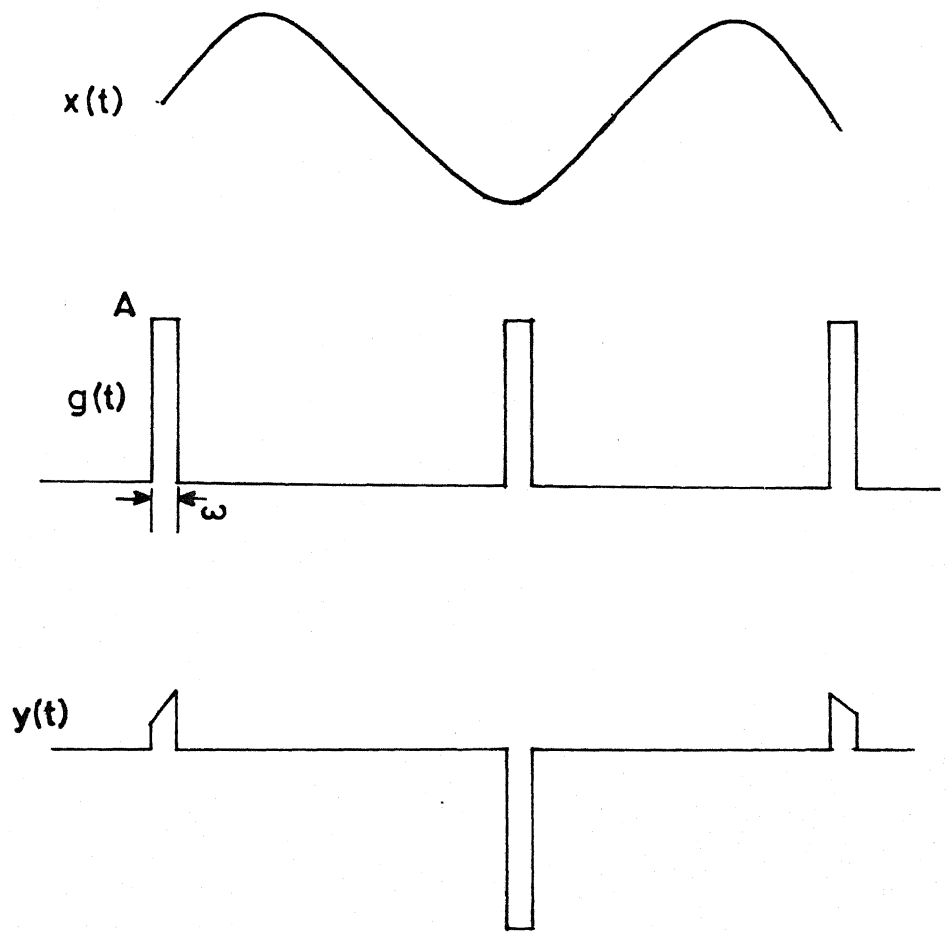


Fig. 4.1 (b) Sampling Action

x(t) is the microwave signal.
g(t) is the conductance of the sampler gate.
y(t) is the output of the sampling circuit.

$$Y(f) = G(f) * X(f) \qquad \ldots(4.2)$$

where * denotes the convolution, given by

$$G(f) * X(f) = \int_{-\infty}^{\infty} G(r)\, X(f-r)\, dr.$$

In order to sample input signals in the GHz frequency range, the sampling pulse function has to be much narrower than the period of the highest frequency required to be sampled. This repetitive pulse train when transformed into frequency-domain gives a line spectrum which is extremely broad with each spectral line corresponding to a harmonic of the pulse repetition frequency. A harmonic converter can also be looked at as a mixer which generates an IF frequency taking the nth harmonic nearest to the signal frequency as LO frequency. But the analysis is not so simple. One needs to take into account the contribution due to the other frequency components as well.

4.2 Sampler

A harmonic converter circuit or a sampler circuit at microwave frequencies uses Schottky diodes as sampling switches, because of the fast switching characteristics required. The narrow sampling pulses are generated using a step recovery diode(SRD).

A schematic diagram of the sampler circuit is shown in fig.4.2. D1 and D2 are the two GaAs Schottky barrier sampling diodes. The sampling drive pulse is applied across the GaAs sampling diodes. Assuming no microwave input signal, the rising edge of the pulse voltage charges capacitors C1 and C2 to the peak pulse voltage through the sampling diodes D1 and D2. Then, as the drive pulse voltage returns to zero potential, the stored capacitor voltage appears across the diodes, reverse-biasing them. Resistor R3, R4 and R5 serve to discharge the capacitors slowly with the output voltage across R_L remaining zero all the time. Now, when a second drive pulse arrives, the GaAs diodes again become forward-biased, provided that the pulse peak voltage is greater

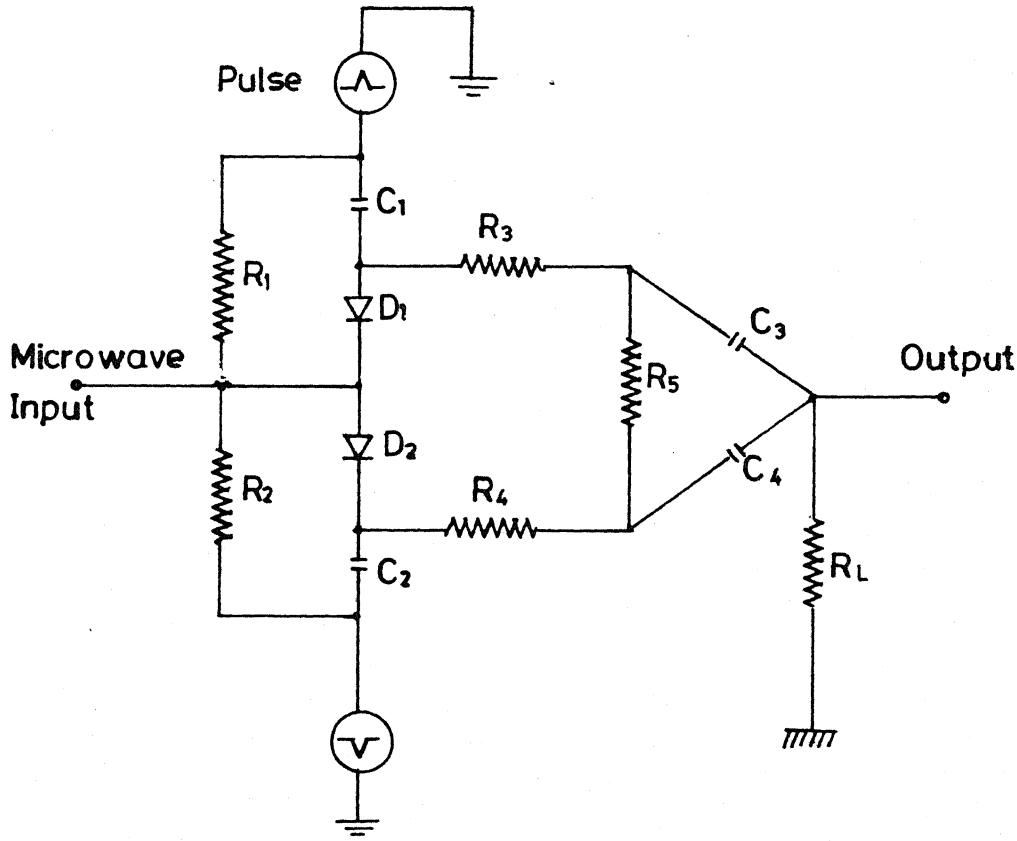


Fig. 4.2 Sampler Circuit.

than the negative self-bias on the diodes.

When a positive voltage is present at the microwave input to the sampler circuit, and the drive pulse is present, then the total current flowing through D2 is slightly more, and the total current flowing through D1 is slightly less, than if no voltage were present at the microwave input. Therefore, capacitor C2 is charged slightly more and C1 is charged slightly less than if no voltage were present at the input. So, a signal voltage appears across the capacitors and causes currents to flow through resistors R3 and R4 and capacitors C3 and C4 to load R_L. If the input signal is negative, similiar operation causes the opposite-polarity signal to appear at the output.

R1 and R2 simply terminate the microwave input transmission line in its characteristic impedance. GaAs diodes are chosen for minimum series resistance, junction capacitance, stray capacitance and inductance to have wide frequency of operation.

4.3 Sampler driver

A SRD is used to generate a narrow sharp triangular pulse. The harmonic generator circuit used for this purpose is shown in fig.4.3. This circuit when driven by a sinusoidal drive signal produces large negative-going triangular pulses of very short duration at the drive frequency. The SRD has a large capacitance under forward bias and a small capacitance under reverse bias. The diode stores the charge during forward bias and when the voltage is reversed,the stored charge starts discharging. When the charge goes to zero, it gives out a very sharp pulse at the output.

In fig.4.3, L_D is the drive inductance and C_T is the tuning capacitance. The section L1 and C1 is used to match the network to the input transmission line characteristic impedance. R_g is the source resistance. In the output of the circuit, SRD is connected to a

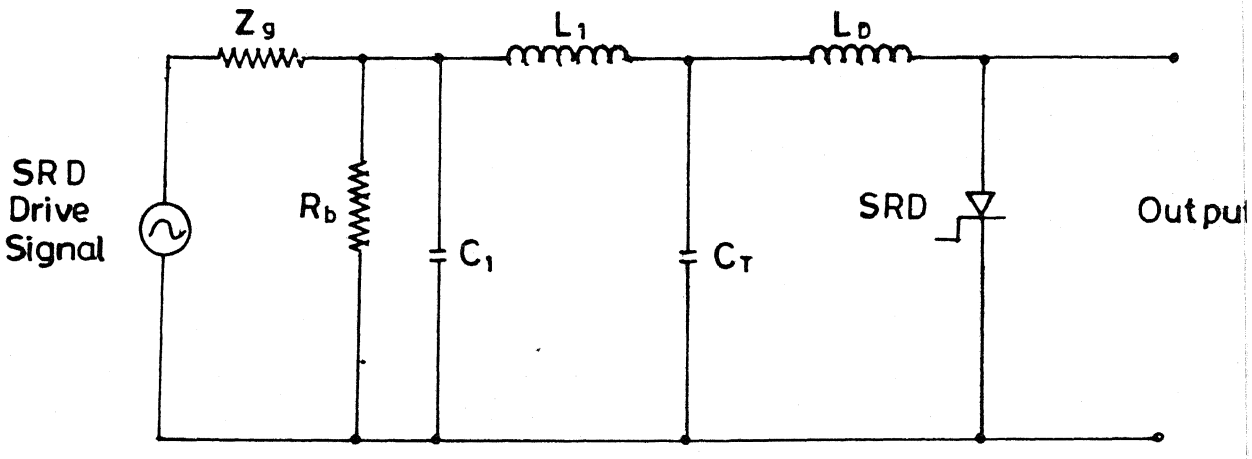


Fig. 4.3 Pulse Generating Circuit Based on a Step Recovery Diode.

microstrip transmission line. The narrow pulse generated by SRD circuit travels along the microstrip line which is coupled to a slot transmission line. The sampling pulse couples to the slotted line through the microstrip, that generates two opposite-polarity pulses to drive the GaAs Schottky barrier diodes (fig. 4.4).

The SRD / Comb generator circuit produces a narrow pulse once per unit cycle, by storing energy in a drive inductance L_D, just prior to the diode capacitance switching from forward to reverse capacitance. This energy appears across depletion capacitance C_d, after switching, as a narrow pulse. The spectral content of the pulse can be found Fourier analysis. Approximating the pulse formed to a triangular pulse of height A, and width w and period T, we have

$$\begin{aligned} f(t) &= 0 ; && -T/2 \le t \le -w/2 \\ &= 2At/w + A ; && -w/2 \le t \le 0 \\ &= -2At/w + A ; && 0 \le t \le w/2 \\ &= 0 ; && w/2 \le t \le T/2. \end{aligned}$$

The Fourier spectrum of this function is then,

$$f(t) = a_0/2 + \sum_{n=0}^{\infty} a_n \cos(2\pi nt/T)$$

where $a_0 = Aw/T$, $a_n = 2AT/n^2\pi^2w\,[1-\cos(n\pi w/T)]$. The amplitude spectrum C_n is given by

$$|C_n| = 2A/n^2\pi^2wf\,[1-\cos(n\pi wf)] \qquad ...(4.3)$$

The first zero occurs at the frequency = 2/w.

The spectrum of sampler driver output for frequencies 900 MHz, 950 MHz and w = 0.045 nsec are shown in fig. 4.5 and 4.6. These figures show that there is power in the harmonics upto 30 GHz.

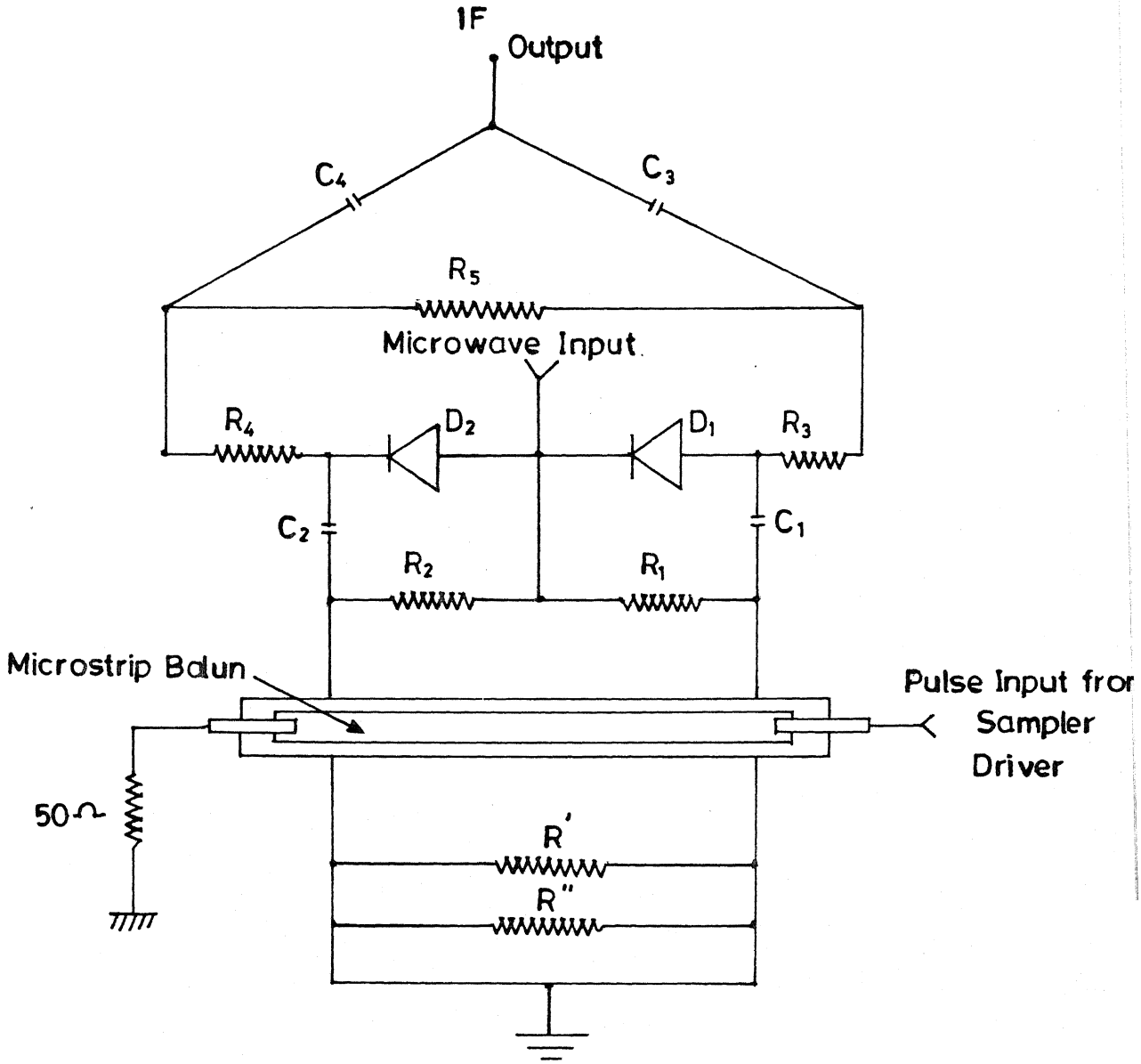


Fig. 4.4 Hybrid Sampler Circuit.

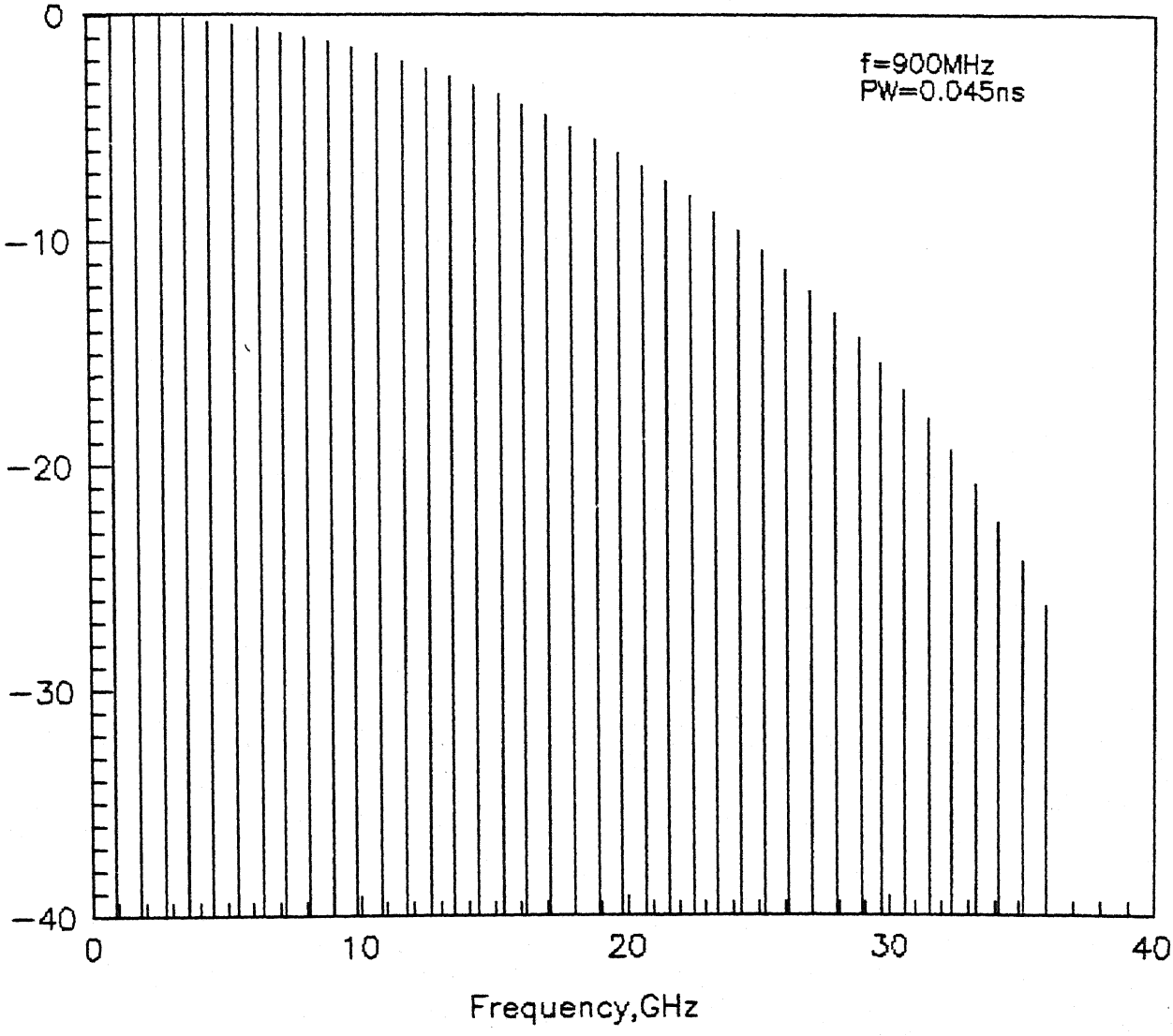


Fig.4.5 Spectrum of a triangular pulse for 900MHz signal

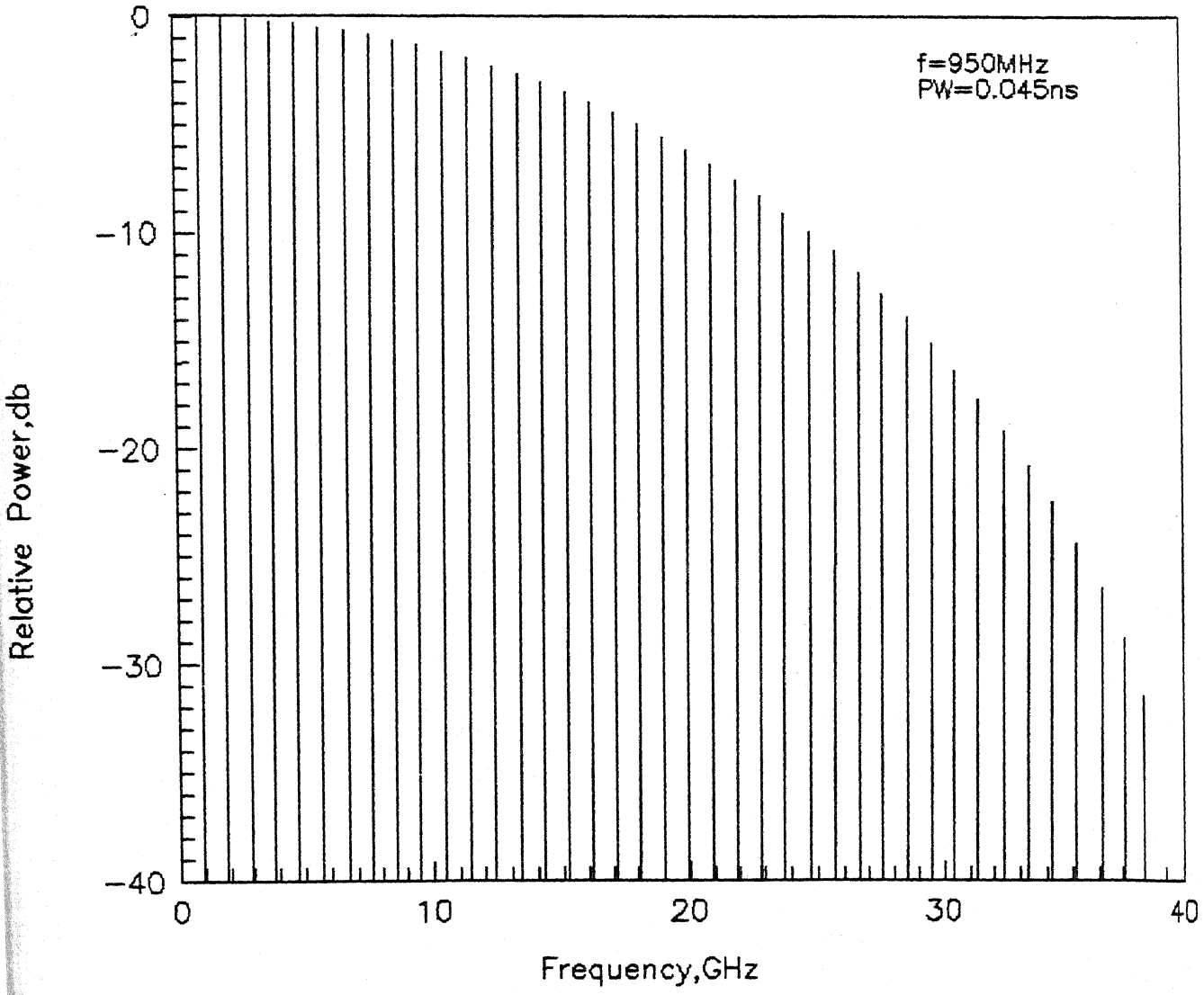


Fig.4.6 Spectrum of a triangular pulse for 950MHz signal

Comb generator circuit design: The design of a comb generator circuit involves 1) Choosing appropriate SRD, 2) Drive inductance L_D, capacitor C_T to tune out at f_i, 3) a matching network (LC section), 4) a bias resistor R_b.

In the depletion or pulse formation interval, the output voltage across SRD is given by [12],

$$e_D(t) = - \frac{I_1\sqrt{L/C}}{\sqrt{1 - \xi^2}} \exp\left[\frac{- \xi\beta t}{\sqrt{1 - \xi^2}}\right] \sin \beta t \qquad ...(4.4)$$

where I_1 is inductor current at the instant of pulse formation.

$$\beta = \sqrt{(1 - \xi^2) / L_D C_D} = \omega_n$$

$$\xi = 1/2R_L \sqrt{L_D/C_D}$$

The pulse width t_p is given by $t_p = \pi/\beta$ ...(4.5)

Drive inductance can be found from t_p as

$$L_D = (t_p/\pi)^2/C_D \qquad ...(4.6)$$

where C_D is the depletion capacitance of the diode.

The tuning capacitor C_T resonates with L_D at f_i, therefore

$$\omega_i L_D = 1/\omega_i C_T$$

From the above equation we have

$$C_T = C_D/(2f_i t_p)^2 \qquad ...(4.7)$$

The load resistor is obtained from ξ as

$$R_L = t_p/2\pi\xi C_D \qquad ...(4.8)$$

For good output and pulse shape ξ is set at 0.3.

The matching network is a two element network. The input impedance at terminals of C_T is a pure resistance R_{in}, which is given by

$$R_{in} \sim \omega_i L_D$$

If R_g is the source impedence and $R_g / R_{in} > 10$, then the values for the matching network are obtained from

$$L_i = X_{Li}/\omega_i = \sqrt{(R_g R_{in})}\,/\omega_i$$

$$C_i = 1/X_{Ci}\omega_i = 1/\left[\sqrt{(R_g R_{in})}\,\omega_i\right] \qquad ...(4.9)$$

The important parameters of SRD are minority carrier life-time, zero bias depletion capacitance, cut-off frequency ($f_{cut-off}$) and parasitic elements.

$$f_{cut-off} = 1/2\pi R_S C_D \qquad ..(4.10)$$

where R_S is the series resistance.The diode with the minimum value of series resistance is chosen for the SRD circuit.

4.4 *Analysis results*

4.4.1 *SRD driver*:

The sampler driver circuit with designed values for input frequency 900 MHz and pulse width 0.045 nsec is shown in fig. 4.7. HP 5082 - 0835 SRD is chosen for the circuit. The parameters for this SRD are $I_S = 0.1 \times 10^{-15}$ A, VT = 26.3 mV, n = 1, M = 0.5, Vj = 0.6, Cjo = 0.5 pf, τ_r = 10 nsec and $R_S = 0.8\ \Omega$. To avoid overflow problems because of the exponential characteristic, the diode characteristic is linearized after 0.8 V. Similarly underflow problem is avoided by limiting the actual characteristic to a linear one at -1 V. The series resistance is

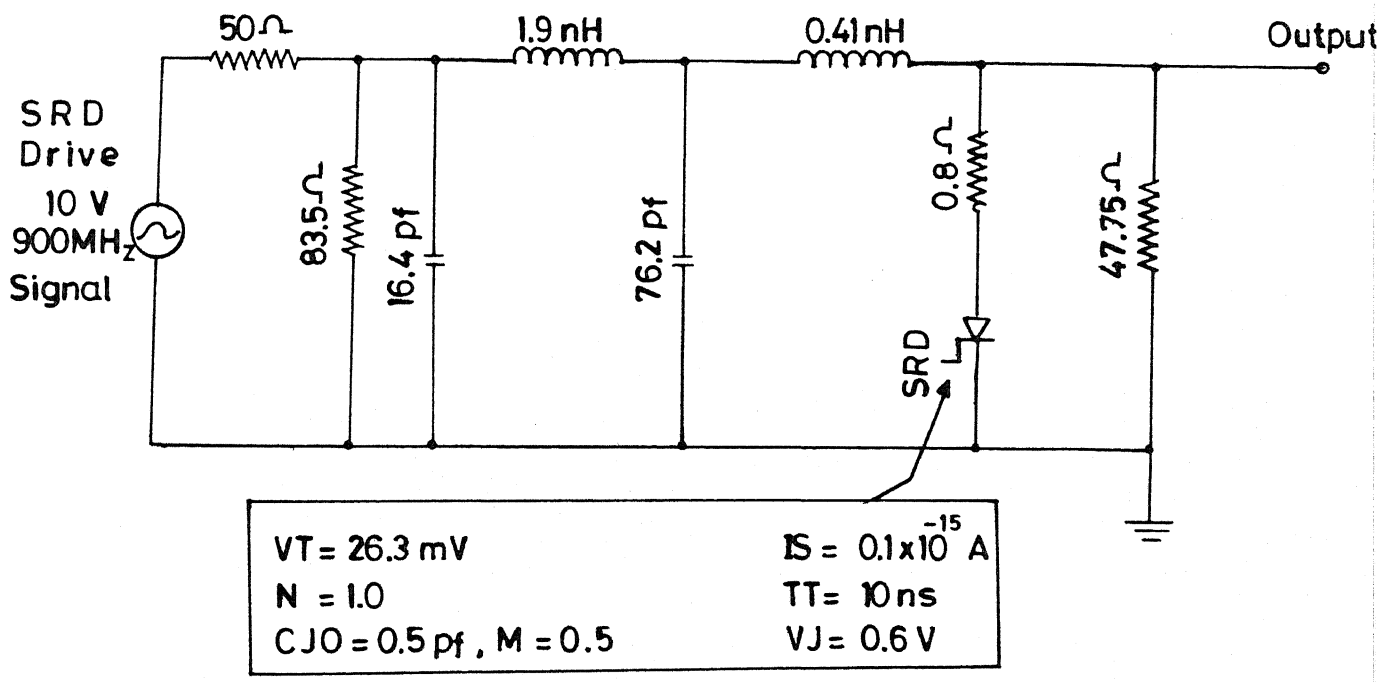


Fig. 4.7 Comb Generator Circuit .

included externally in the model for SRD. A time step of 0.1 nsec was chosen for the circuit. The calculated output waveform for many periods is shown in fig. 4.8. Similarly the SRD circuit has been solved for a input frequency of 950 MHz and pulse width 0.045 nsec. The calculated output waveform for this designed circuit is shown in fig. 4.9. The input format for this circuit is given in Table 4.1.

4.4.2 *Sampler circuit*

The sampler circuit with element values is shown in fig. 4.10. A GaAs diode (HP 5082 - 0087) with parameters I_s = 0.75 nA, VT = 26.3 mV, n = 1, M = 0.5, Vj = 0.2 V, Cjo = 1 pf and R_s = 12 Ω has been chosen . To avoid overflow problems, the diode dc characteristic is linearized at 0.3 V. The analysis of this circuit gave convergence problem. To avoid this, the junction capacitance of the diode has been taken as a fixed value of 1 pf. A time step of 0.005 nsec was chosen for this circuit. The circuit has been analysed upto 10 nsec. The input signal is varied from 1 to 24 GHz. Simultaneously, the SRD drive signal is also varied from 900 to 975 MHz so that the IF signal frequency is always fixed at 100 MHz. The IF signal frquency is given by

$$f_{IF} = f_{Sig} - nf_O$$

where f_{Sig} is the input signal frequency, f_O is the drive frequency and n is the harmonic of drive signal.

The computed IF output waveforms for different input frequencies 1, 2, 8, 24 GHz are shown in figs. 4.11, 4.12, 4.13 and 4.14 respectively. The input format for this circuit is shown in Table 4.2. The conversion gain at different frequencies has been calculated and shown in fig. 4.15.

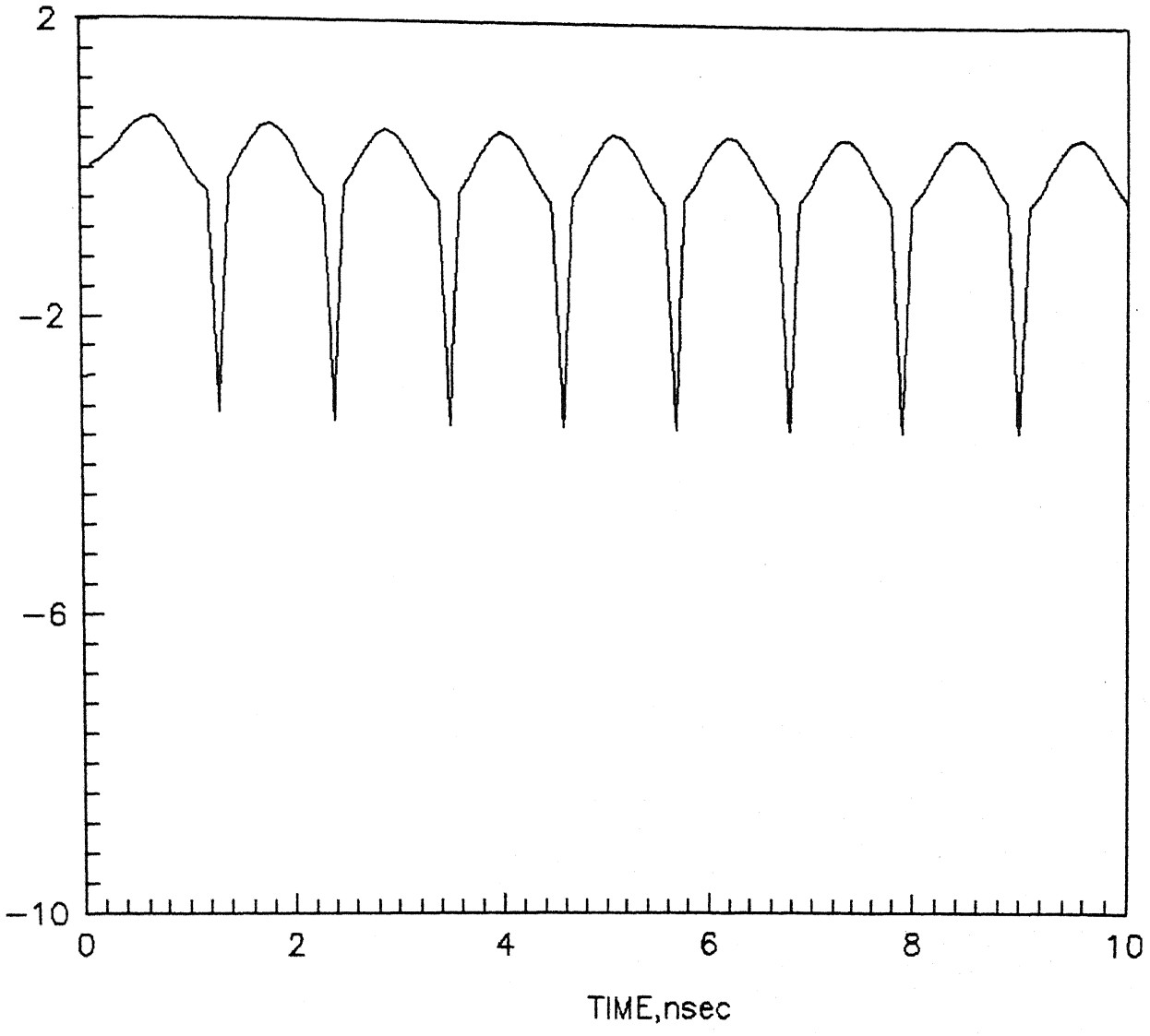


Fig.4.8 Sampler driver output voltage waveform (900MHz drive signal)

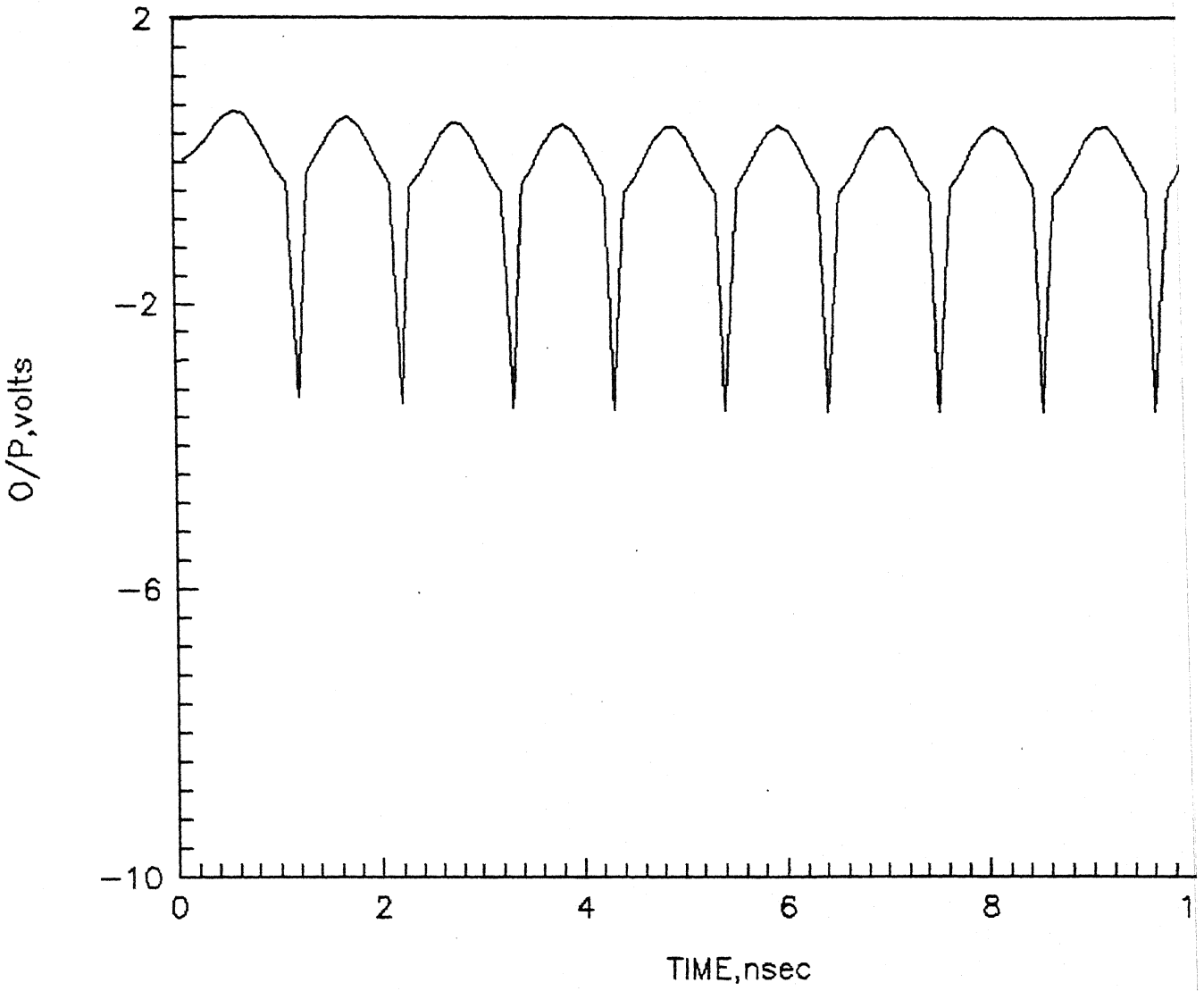


Fig.4.9 Sampler driver output voltage waveform (950MHz drive signal)

```
100
RCLVPDS
 10   6   1   0   1   0.1E-09
V   1   0
0.1E02      0.95E09
R   1   2
0.5E02
R   2   0
0.931E02
C   2   0
0.151E-10
L   2   3
0.185E-08
C   3   0
0.684E-10
L   3   4
0.41E-09
R   4   0
0.4775E02
R   4   5
0.8E00
S   5   0
0.1E-15    0.263E-01 0.1E01     0.5E00      0.6E00      0.5E-12    0.1
```

Table.4.1 Input format for pulse generating circuit

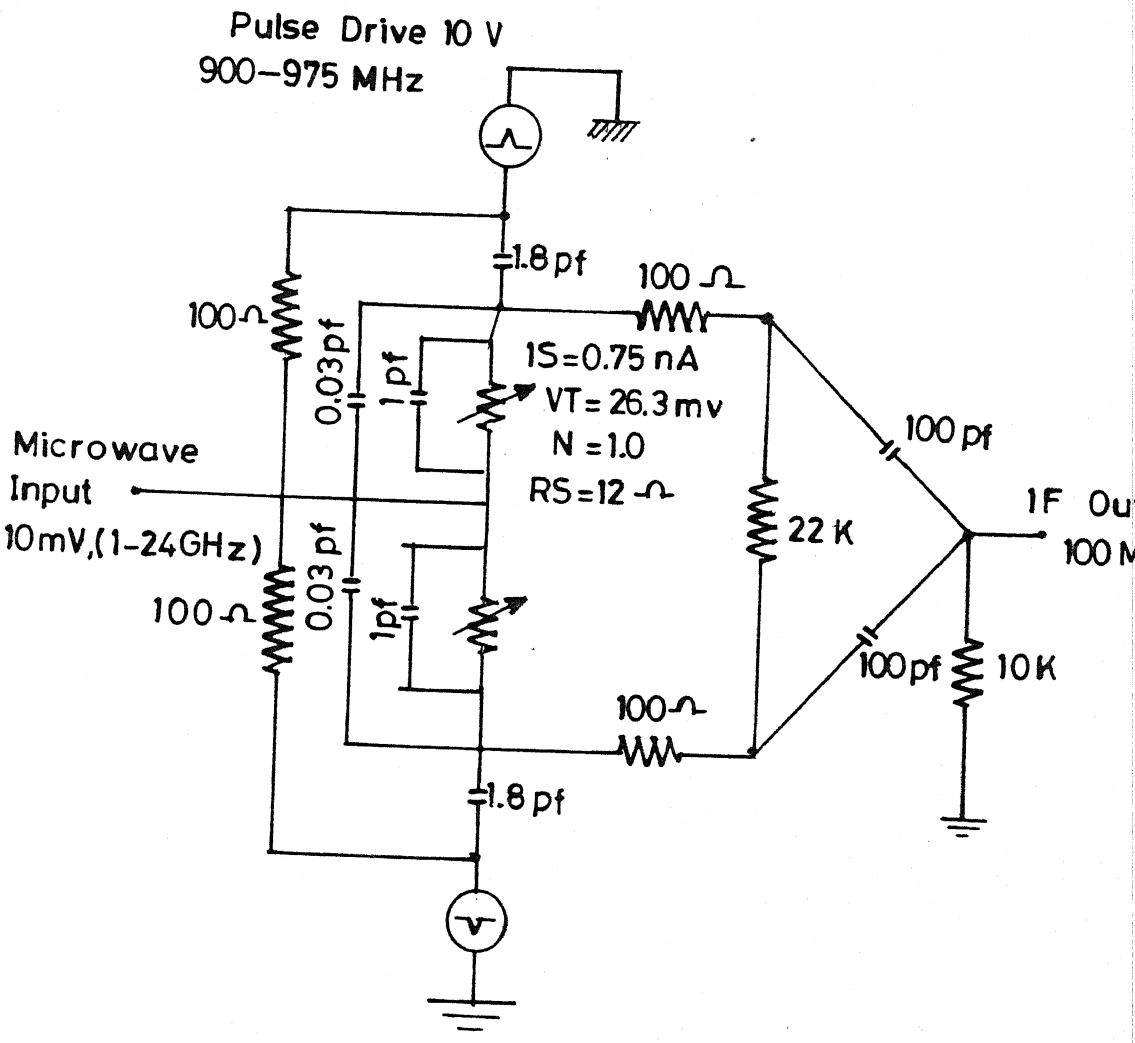


Fig. 4.10 Sampler Circuit.

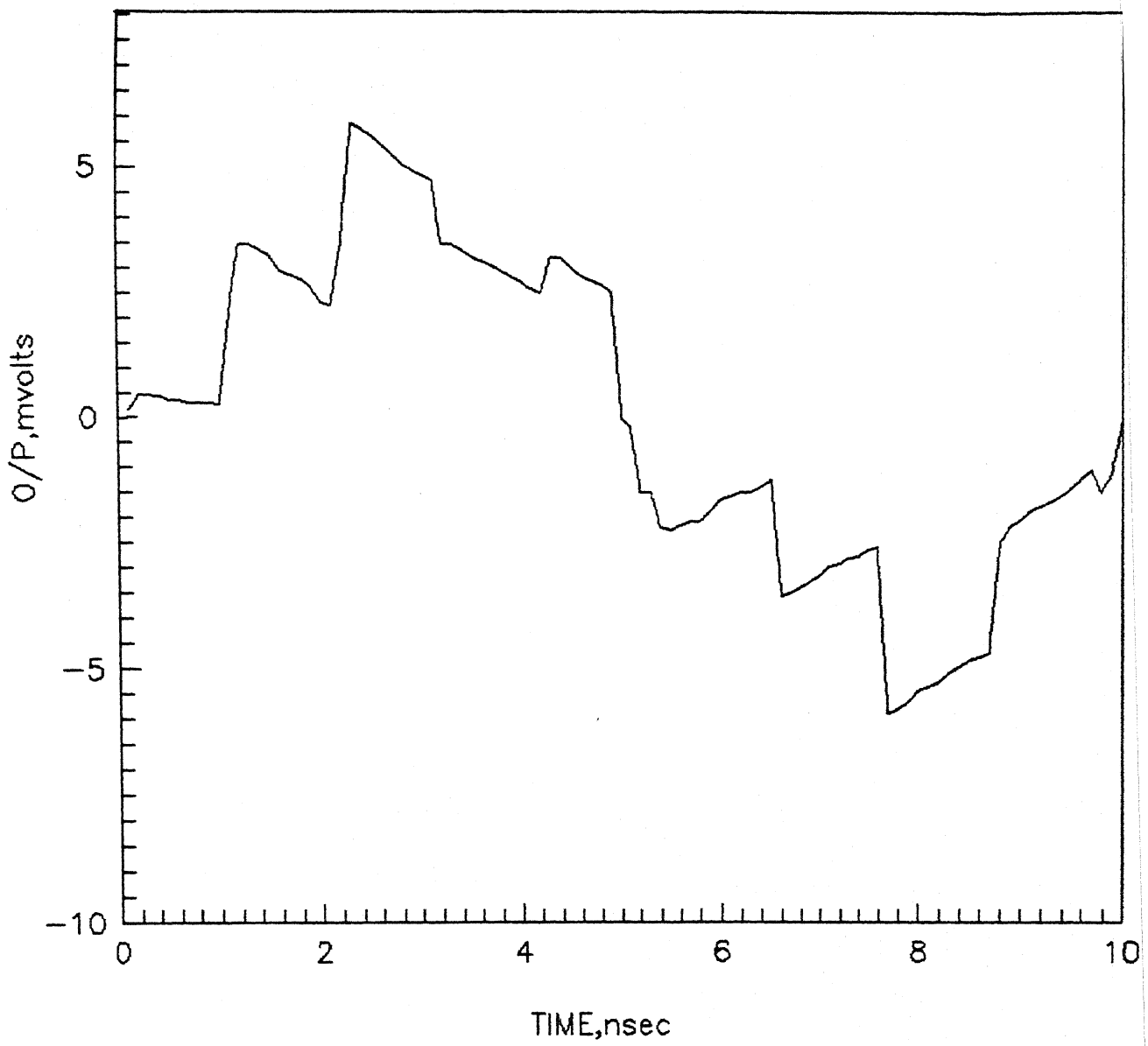


Fig.4.11 Sampler output voltage waveform for 1GHz input signal

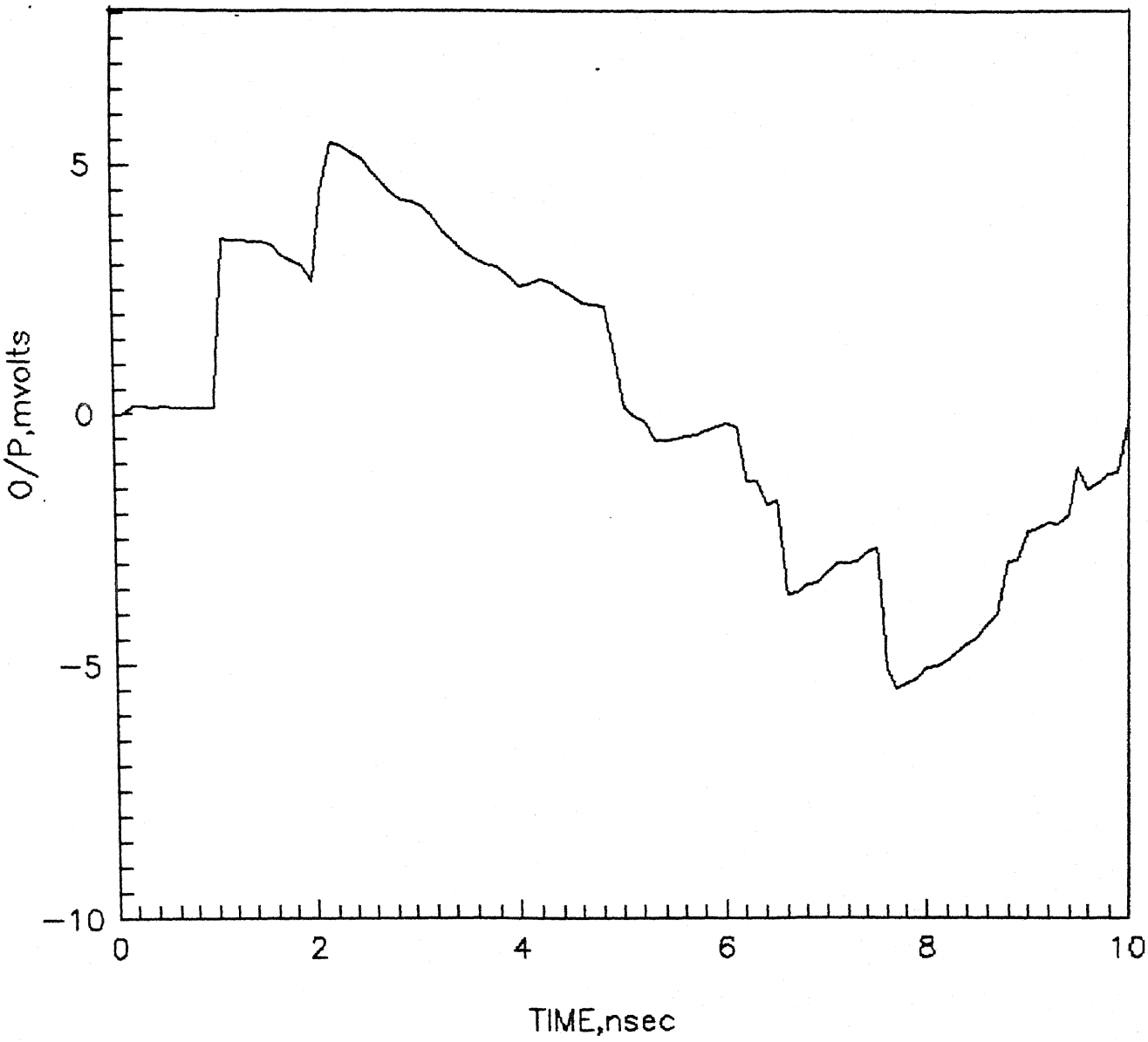


Fig.4.12 Sampler output voltage waveform for 2GHz input signal

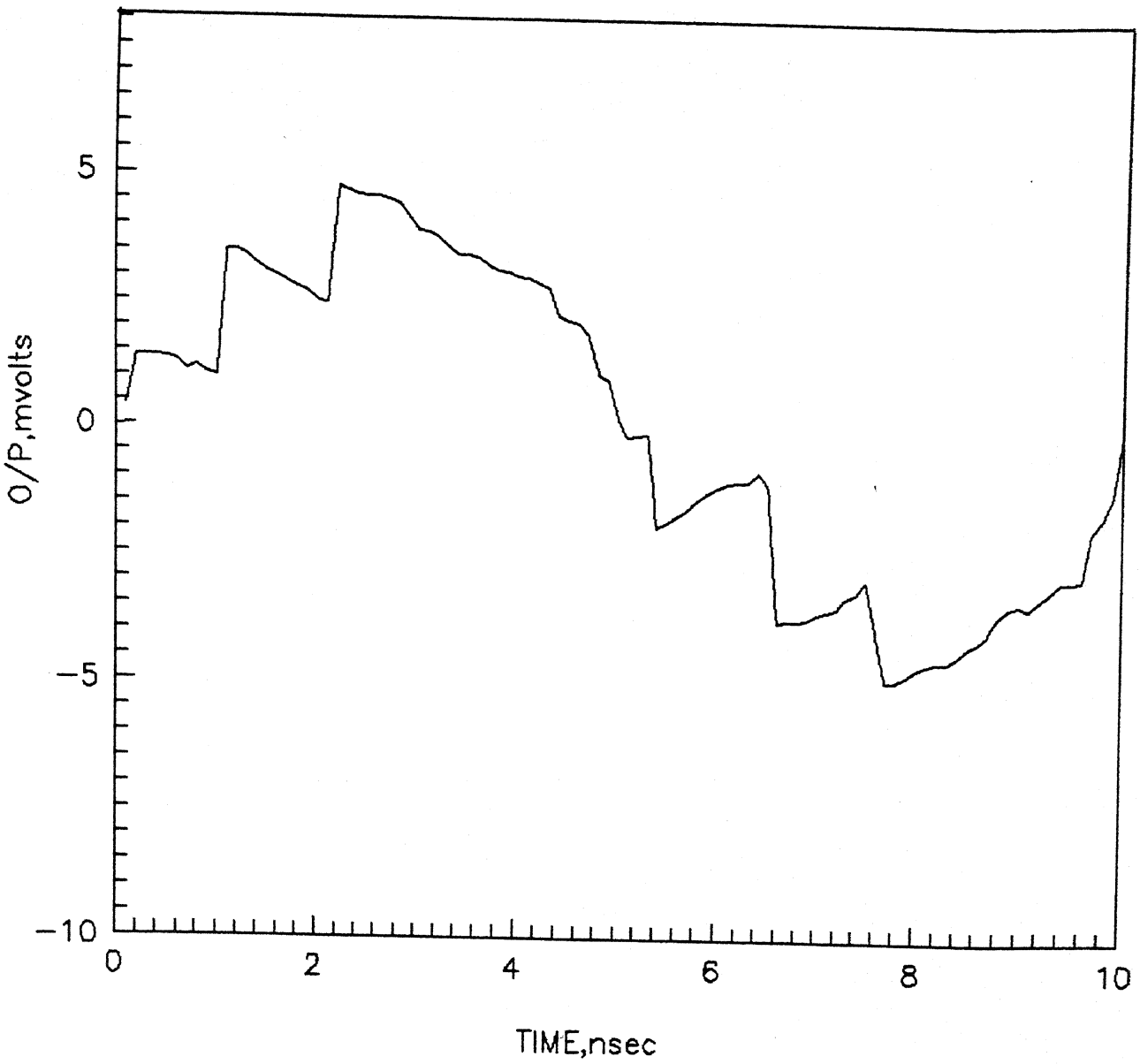


Fig.4.13 Sampler output voltage waveform for 8GHz input signal

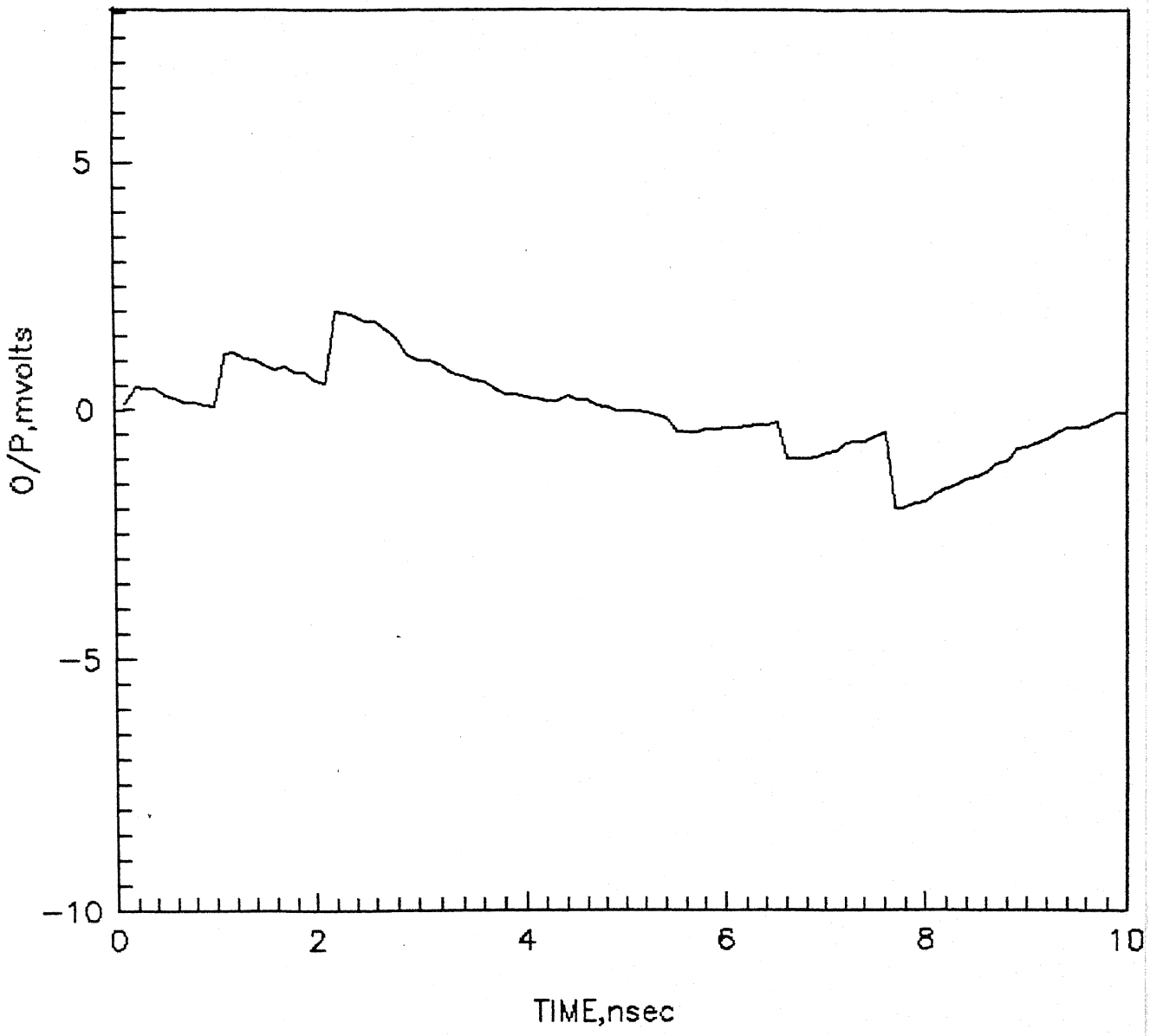


Fig.4.14 Sampler output voltage waveform for 24GHz input signal

```
2000
RCLVPDS
 18   9   3   2   0   0.5E-11
V   1   0
0.1E-01     0.1E10
P   2   0
0.1E02      0.9E09      0.45E-10
P   3   0
-0.1E02     0.9E09      0.45E-10
R   4   6
0.1E03
R   5   7
0.1E03
R   6   7
0.22E05
R   8   0
0.1E05
C   2   4
0.18E-11
C   3   5
0.18E-11
C   6   8
0.1E-09
C   7   8
0.1E-09
C   1   4
0.3E-13
C   1   5
0.3E-13
C   1   4
0.1E-11
C   1   5
0.1E-11
D   4   1
0.75E-09   0.263E-01 0.1E01     0.5E00     0.2E00     0.2E-11    0.1
D   1   5
0.75E-09   0.263E-01 0.1E01     0.5E00     0.2E00     0.2E-11    0.1
```

Table 4.2 Input format for sampler circuit

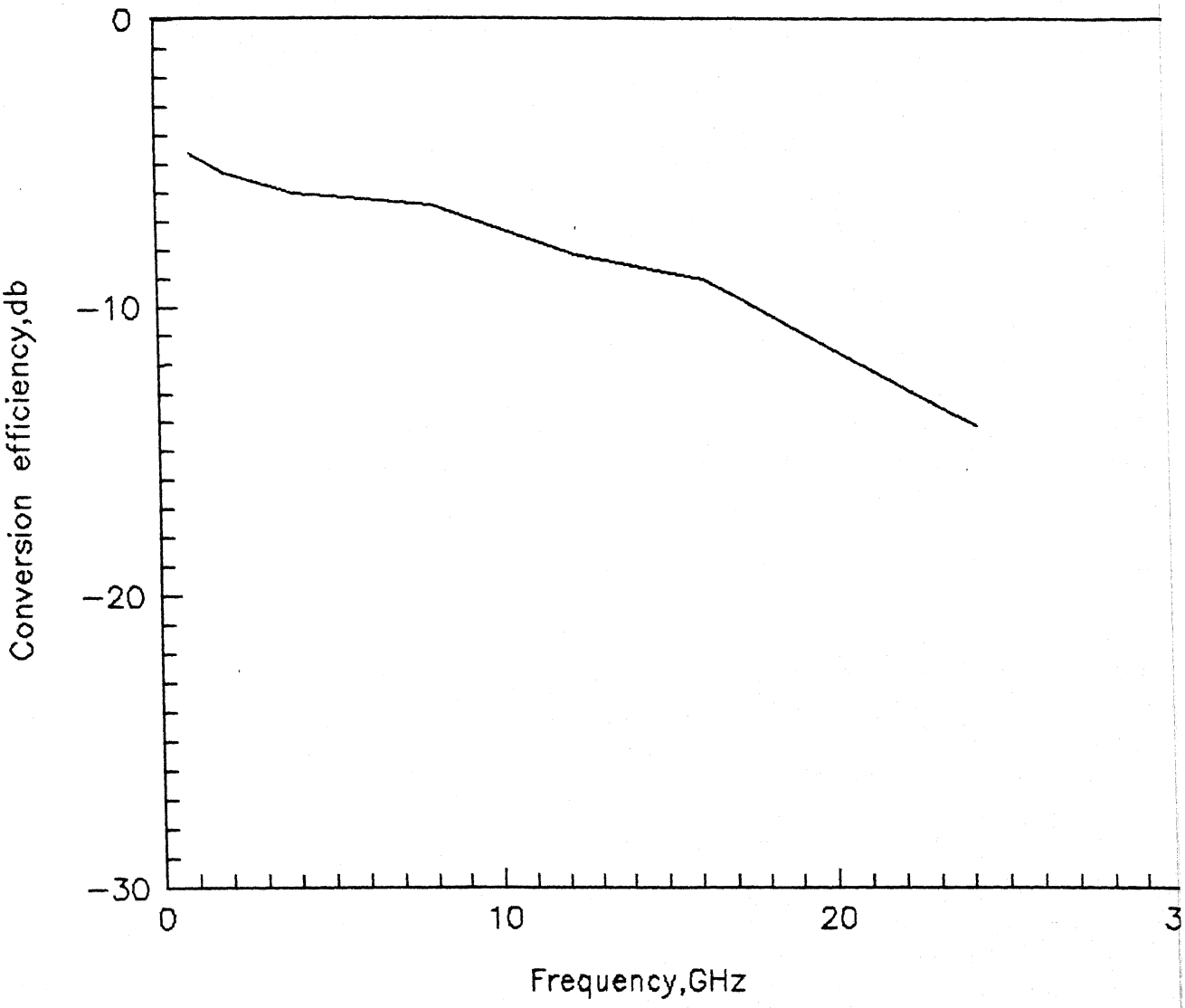


Fig.4.15 Conversion efficiency of a sampler circuit

5. DESIGN OPTIMIZATION

5.1 *Introduction*

In any circuit or system design it is desirable that the circuit is not only functional but also optimum. The first task in optimization is to define what is optimum. This generally depends on the system and to some extent on the application. For example, we can define an optimum amplifier as the one that gives maximum gain while retaining the necessary bandwidth. It is well known that the Gain-Bandwidth product is constant in an amplifier, therefore maximum gain always occurs when the bandwidth is just sufficient or equal to that required by the constraint. Now, this can be a criteria of optimization in the case of an amplifier used as a power amplifier. But, if we are using the amplifier as the first stage of a receiver which contributes maximum to the degradation of signal-to-noise ratio, the optimality criteria is better chosen to be one of lowest noise figure subject to the bandwidth constraint. Thus, the criteria of optimization can depend on the application.

Generally, two kinds of problems are encountered in an optimization process. One is the unconstrained and the other constrained optimization. The unconstrained problem is generally one of finding a maximum or minimum of a function. The procedure is to define an objective function which is minimized. (Maximization can be treated as minimizing the negative of the objective function.)

The constrained optimization problem is normally solved by first converting the problem to an unconstrained one. This is done by constructing the objective function which includes the constraints automatically. There are several methods for doing this. The choice of the method depends on the problem and the type of constraints.

Now, looking at the methods of minimization, one comes across a large number of algorithms, each one best suited for certain type of

problems or objective functions. The methods can be classified mainly into two categories, methods based on gradients and numerical search methods. Of course, the discussion here is confined to nonlinear function minimization. Linear functions are best minimized using the linear programming methods.

All the gradient methods are based on the Taylor series expansion of the function about the minimum point. The drawbacks of these methods is the requirement of computation of gradients or the derivatives and their tendency to obtain local minimum or the minimum nearest to the starting point. There are some algorithms, such as Fletcher Powell algorithm, which do away with gradient computation but still suffer from the second drawback.

When the objective function is well behaved smooth function or nearly a quadratic function, gradient methods perform very well, provided the initial point can be properly chosen. But when the objective function is complicated with large number of local minima, some of the numerical search techniques perform much better. Although, there is no sure shot way of determining global minimum, the probability of hitting a global minimum can be said to be higher in some of the numerical search techniques.This, of course, is a qualitative statement supported only by experience.

From these reasonings, a nonlinear minimization algorithm known as 'simplex method' developed by Nelder and Mead [33] was chosen for optimizing the harmonic converter circuit. A brief description of the method is given later in this chapter.

As mentioned earlier in this section, the first task in finding an optimum solution or design, is to define or construct an objective function. All the literature on optimization deals with the problem of searching for the minimum, given an objective function ; and also deals

with how to convert a constrained problem to an unconstrained one. Therefore, the task of defining an optimum criteria and formulating an objective function is left to the individual, who is trying to design an optimum system, and is the best judge to decide on these matters, as he knows the system best.

One of the major difficulties faced in the present problem of optimizing a harmonic converter circuit design is the computational time required. All the optimization algorithms are in general search for the minimum of the objective function iteratively, although search strategy is different in different methods. In order to reduce the computational time it is desirable that the objective function computation is fast and the number of function evaluations or iterations be minimum. The number of iterations required to find a minimum of the function depends on the minimization algorithm as well as the function behaviour with respect to the variables of optimization. The specific problem faced in optimizing harmonic converter circuit is one of inordinately large time for function computation.

An important parameter of a harmonic converter is its conversion loss. It was sought to minimize the conversion loss by appropriate choice of component values. Therefore, the objective function would logically be the conversion loss and the circuit elements as the variabes of optimization. Now, to express conversion loss in terms of element values is not simple; in fact, complete time-domain analysis as developed in earlier chapters has to be gone through for several time steps to construct the output signal, in terms of which the conversion loss is defined. This takes large computational time.

In order to reduce the computational time, it is desirable to reformulate the objective function. What is attempted in this thesis is to define a new function which in some way related to the conversion loss; and it is hoped that by optimizing this new parameter, which takes much less time to compute, we are actually minimizing the conversion

loss. There is no proof provided to show that this really happens. Instead of computing the output waveform once several time steps and then finding the maximum or the rms value of that waveform ,a single sample value at a time step just after the sample pulse amplitude goes to zero is used in the objective function. The ratio of the input voltage at the sampling instant to the sampled output voltage value is taken to be some representative of the conversion loss. By heuristic reasoning one can see that this ratio in some way directly related to the conversion loss and minimizing this ratio, we are actually minimizing the conversion loss in some indirect way.

5.2 *Objective function and variables of optimization for sampler circuit.*

The function of the sampler is to convert microwave frequencies to IF frequencies with minimum signal loss. So, objective function for sampler circuit is the conversion loss. The objective function is defined as

$$F = \frac{V^2_{max,input}/Z_O}{V^2_{max,output}/R_L} \qquad \ldots(5.1)$$

where Z_O is the characteristic impedance of the input line and R_L is the load resistance.

The ideal diode for sampler circuit is a diode with zero series resistance, parasitic elements and zero cut-off potential. So, a GaAs diode with minimum series resistance, parasitic elements has been chosen. The parameters for the variables of optimization process taken are R3, R4 and R5. The SRD drive input with minimum pulse width gives flatter frequency response, but greater conversion loss.

The determination of conversion loss function in the analysis involves a nonlinear problem. The behaviour of the objective function is totally unknown and is highly nonlinear. It can have multiple minima. Such functions don't easily yield to gradient methods because, these methods generally give the minimum nearest to the starting point, near

the global minimum which is often difficult in the case of nonlinear functions.

5.3 *Numerical search algorithm for function minimization*

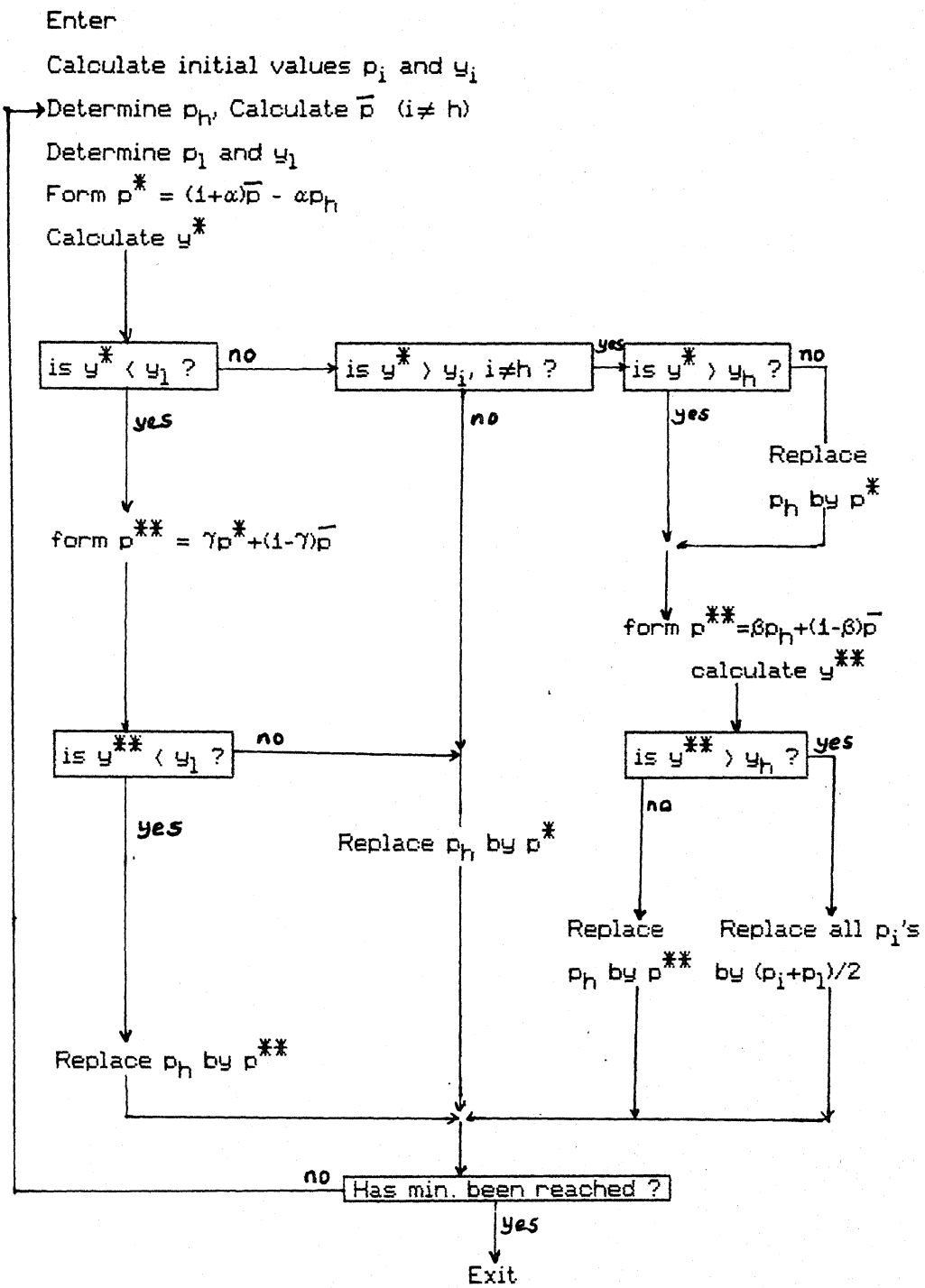
The geometrical figure formed by a set of (n+1) points in an n-dimensional space is called a simplex. The 'n' points forms a set of variables of optimization.

The objective function formulation for conversion loss is nonlinear and can have multiple minima. The simplex search method of Nelder and Mead [33] which is a powerful method in handling nonlinear functions has been used in this thesis. This method has multiple starting points and has greater probability of locating the global minimum. This starts with a set of (n+1) points, termed simplex, the next iterative point being formed by reflecting the point with the highest objective function value about the centroid of the rest of the n-points. The line joining the centroid and the point with the highest function value gives the general direction in which the function decreases and the simplex is expanded or contracted in the direction depending on the function value of the new calculated point. The search is terminated when the difference between the highest and the lowest function values, among the points of the simplex, is less than a pre-specified value.

5.4 *Computational aspects of minimization*

The evaluation of the objective function formulated as in eqn.(5.1) takes large time, that is, around 38 minutes in PC/XT, for a single function evaluation. So it is not practically possible to implement this. Therefore a time point after the SRD drive signal falls to zero in the first cycle is assumed to represnt the maximum value of the output, IF signal. The objective function is then defined as

$$F = \frac{V^2_{input}(\text{at } 0.05 \text{ ns})/Z_0}{V^2_{output}(\text{at } 0.05 \text{ ns})/R_L} \qquad \ldots(5.2)$$



$\alpha = 1$

$\beta = 0.5$ ((1)

$\gamma = 2.0$ ()1)

Fig. 5.1 Simplex algorithm

which is a representative of the conversion loss in some indirect way.

The variables for the optimization taken are R3, R4 and R5. The search simplex is formed around the point (R3 = 100Ω, R4 = 100Ω, R5 = 22 K) by symmetrically perturbing each component by a fixed amount to give a new point. In the process of function minimization, the variables R3, R4 and R5 may go to negative value. Whenever the variable is going to negative value, the variable is changed to some positive value and the process is continued (R3, R4 and R5 are taken as 10Ω, 10Ω, 22K respectively). The minimization is terminated when $|y_h - y_l| < 0.001$ is obtained. The process took 26 iterations for minimization. The optimized variables are R3 = 12.4 Ω, R4 = 12.4 Ω and R5 = 27.95 K for 1 GHz input signal. The objective function value in dB for the optimized sampler circuit is 4.55 dB for 1 GHz input signal.

The elements C1 and C2 are also taken as variables and tried in the simplex program, but the objective function behaved randomly and we could not get the minima for this case.

5.5 Conclusion and discussions

The iteration time in the optimization process is found to depend on the constraint level .The number of iterations also depend on the number of variables.

The Schottky diode with minimum series resistance and parasitic elements was chosen .The ideal diode for the sampler circuit can be easily determined and so the diode parameters were not included as optimization variables.Also,for SRD driver circuit,the output voltage has to be a delta function for generating a narrow sharp triangulur pulse and it can be obtained if the depletion capacitance of the diode is too small and the forward diffusion capacitance is high .Therefore the pulse generating circuit was not optimized .

6. CONCLUSION AND SCOPE FOR FURTHER WORK

6.1 *Present work*

In this thesis, a time-domain method for nonlinear microwave circuits has been suggested and successfully applied to harmonic converter circuit. The method is efficient for solving a class of strongly nonlinear microwave circuits and/or input signals having a large number of harmonics. The system matrix is formulated using nodal analysis and the matrix diagonal elements are all strong. The input source variables are avoided by the present formulation. The method requires only one matrix inversion per time step.

The modelling of Schottky diode and step recovery diode have been discussed. Also the modelling of lossy dispersive transmission line is discussed. The harmonic converter circuit has been solved by the present method and results have been obtained for different frequencies. Finally, a possible application of function minimization algorithm to optimize the performance of the circuit has been discussed.

6.2 *Limitations of the present method and scope for further work*

The present time-domain method requires a convergence criteria as discussed in the section 2.4.3. This condition, sometimes, is difficult to satisfy. So, present method fails for those nonlinear circuits, for which convergence criteria cannot be satisfied. Under these circumstances, one or more Newton-Raphson iterations can be applied, whenever the present iteration process diverges.

The transmission line (lossy and dispersive) model has not been included in the present work. This model can be included and a wide class of microwave circuits can be analyzed. Also, models for other nonlinear devices such as PIN diode, Varactor, Tunnel diode, Gunn diode and MESFET can be included in the program.

APPENDIX-A

Device Physics

1. GaAs Schottky barrier diode

i) Depletion or junction capacitance: The space charge layer width of a Schottky barrier on a uniformly doped n-type GaAs semiconductor is

$$X_d = \sqrt{\frac{2\epsilon(\phi - v)}{qN_d}}$$

where ϵ is the permittivity of the GaAs semiconductor, N_d is the doping density, ϕ is the contact potential and v is the reverse bias voltage. The capacitance of the junction is therefore given by

$$C_j = \frac{\epsilon A}{X_d} = \sqrt{\frac{q\epsilon N_d}{2(\phi - v)}}\, A$$

where A is the area of the diode. The above equation can be written as

$$C_j = \frac{C_{jo}}{\sqrt{(1 - v/\phi)}}$$

where $C_{jo} = \sqrt{\frac{q\epsilon N_d}{2\phi}}\, A$.

2. Step recovery diode

i) Diffusion or forward capacitance : In the forward biased condition, the charge in the p-region of SRD is given by

$$Q_p = qAL_p p_{no} (\exp(v/nV_T) - 1)$$

and the charge in the n-region is given by

$$Q_n = - qAL_n n_{po} (\exp(v/nV_T) - 1)$$

where q is the electronic charge, A is the area of the diode , L_p and L_n are the diffusion lengths for holes and electrons, p_{no} and n_{po} are the minority hole and electron concentration in n and p-regions respectively, $V_T = KT/q$ and n is the ideality factor. The total diffusion charge is then given by

$$Q_{diff} = Q_p + | Q_n | = - qA(L_n n_{po} + L_p p_{no}) (\exp(v/nV_T) - 1)$$

Therefore diffusion capacitance is

$$C_D = dQ_{diff}/dv = \frac{qA(L_n n_{po} + L_p p_{no}) \exp(v/nV_T)}{nV_T}$$

If $p_{no} \gg n_{po}$, $C_D \approx \frac{qAL_p p_{no} \exp(v/nV_T)}{nV_T}$

or this can be written as

$$C_D = (I_S \tau_p/nV_T) \exp(v/nV_T)$$

where $I_S = qAD_p p_{no}/L_p$ and $\tau_p = L_p^2/D_p$. τ_p is the life time for holes in the n-region and D_p is the diffusion constant for holes.

ii) Depletion or transition capacitance : The charge in the space charge layer during reverse bias condition is given by

$$Q_j = A \sqrt{2\epsilon_{Si} q \left[\frac{N_A N_D}{N_A + N_D}\right] (\phi - v)}$$

where A is area of the junction, ϵ_{Si} is the permittivity of silicon, ϕ is the contact potential, N_A is the acceptor concentration in p-region, N_D is the donor concentration in n-region and v is the applied reverse bias.

The transition/depletion capacitance is therefore given by

$$C_T = \frac{d\phi_j}{dv} = A \sqrt{\epsilon_{Si} q \left[\frac{N_A N_D}{N_A + N_D} \right] \frac{1}{2(\phi - v)}}$$

or can be written as

$$C_T = \frac{C_{jo}}{\sqrt{(1 - v/\phi)}}$$

where C_j is the zero bias capacitance.

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